Exhibit A

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571-272-7822

Paper 13
Date: April 12, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-01428
Patent 8,787,060 B2

Before PATRICK M. BOUCHER, DANIEL J. GALLIGAN, and SHEILA F. McSHANE, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Samsung Electronics Co., Ltd. ("Petitioner") filed a petition for *inter partes* review (Paper 1 ("Pet." or "Petition")) challenging claims 1–34 of U.S. Patent 8,787,060 B2 (Ex. 1001 ("'060 patent")). Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). With our authorization, Petitioner filed a Reply to Patent Owner's Preliminary Response (Paper 9 ("Reply")), and Patent Owner filed a Sur-reply to Petitioner's Preliminary Reply (Paper 10 ("Sur-reply")).

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review. The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons explained below, we institute an *inter partes* review of all challenged claims on all grounds raised in the Petition.

B. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including IPR2022-01427, which involves related Patent 9,318,160 B2, which is a continuation of the '060 patent. Pet. 1; Paper 3 at 1.

C. Real Parties in Interest

Petitioner identifies itself and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 1. Patent Owner identifies itself as the real party in interest. Paper 3 at 1.

D. The '060 Patent and Illustrative Claim

The '060 patent relates to computer memory devices and, more specifically, to reducing the load of drivers in memory. Ex. 1001, 1:18–21. As background, the '060 patent describes an existing memory package with reference to Figure 1A, reproduced at right, which shows memory package 100 with control die 130 and three array dies 110. Ex. 1001, 1:30–44. Control die 130 has driver 134, which drives data signals from control die 130 to each array die via interconnect 142, and driver 140, which drives command and address signals to each array die. Ex. 1001, 1:35–42. The '060 patent explains that "a load exists on each of the drivers 134, 140 . . . by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies." Ex. 1001, 2:8–11. The '060 patent discloses that, "to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver" and that "a larger driver not only consumes more space on the control die, but also consumes more power." Ex. 1001, 2:11–15.

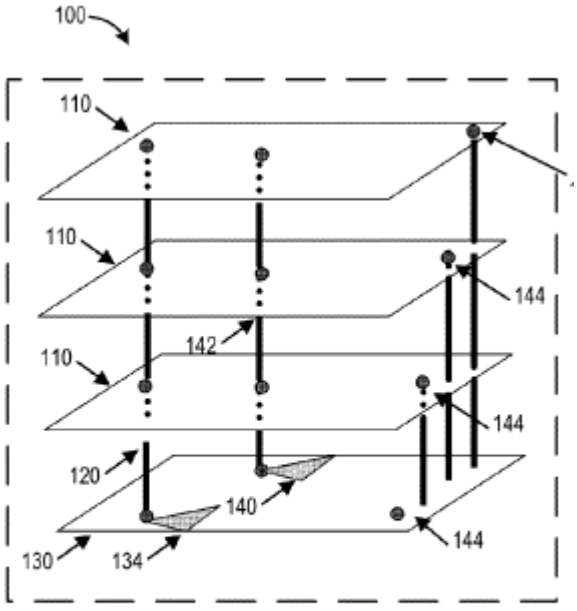


FIG. 1A

The '060 patent proposes that driver size and power consumption can be reduced "by increasing the number of die interconnects and reducing the number of array dies that are in electrical communication with each die

interconnect." Ex. 1001, 4:22–26. The '060 patent illustrates an exemplary configuration in Figure 2, reproduced at right, which shows memory package 200 with control die 230 and four array dies 210a–210d. Ex. 1001, 5:12–13. Control die 230 is connected to array dies 210a and 210b by die interconnect 220a, as shown by the darkened circles. Ex. 1001, 5:63–6:1. Die interconnect 220b connects control die 230 to array dies 210c and 210d, as shown by the darkened circles, but die interconnect 220b is not electrically connected to array dies 210a and 210b, as shown by the unfilled circles. Ex. 1001, 6:9–23. Thus, in the disclosure of Figure 2, the die interconnects do not connect to each array die as in Figure 1A discussed above.

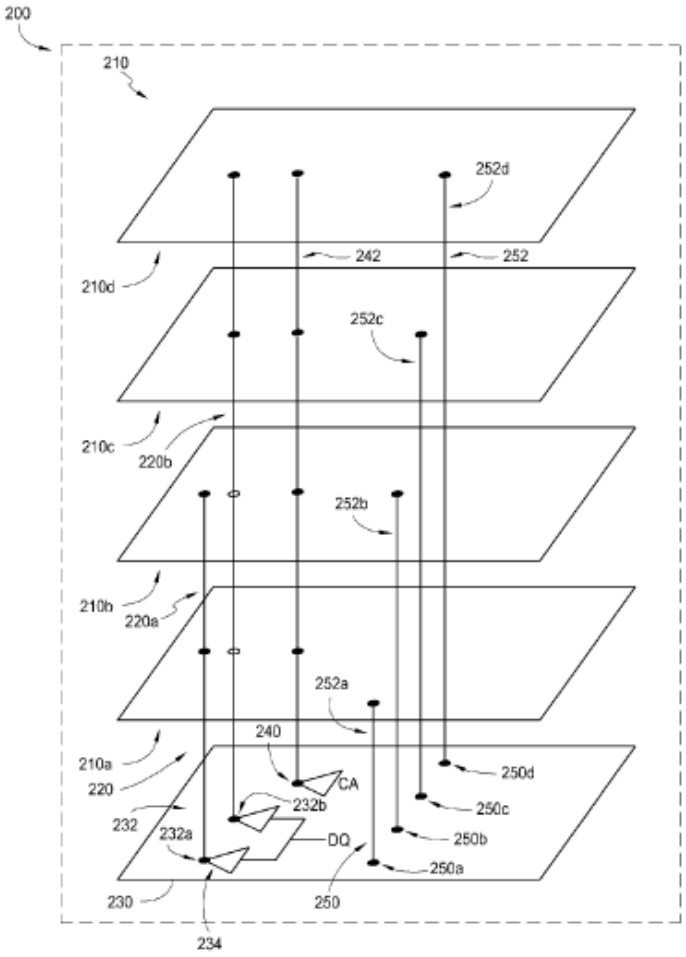


FIG. 2

Claim 1 is illustrative and is reproduced below with Petitioner's claim element identifiers in brackets.

1. [1.a] A memory package, comprising:

   [1.b] a plurality of input/output terminals via which the memory package communicates data and control/address signals with one or more external devices;

[1.c] a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports;

[1.d.1] at least a first die interconnect and a second die interconnect, the first die interconnect in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [1.d.2] the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

[1.e.1] a control die comprising [1.e.2] at least a first data conduit between the first die interconnect and a first terminal of the plurality of input/output terminals, [1.e.3] and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, [1.e.4] the control die further comprising a control circuit to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals.

E. Asserted Grounds of Unpatentability

Petitioner presents the following grounds (Pet. 3):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–6, 8–14, 16–19, 29–34	103(a)	Kim,[1] Rajan,[2]
1–14, 16–19, 29–34	103(a)	Kim, Rajan, Riho,[3]
1–6, 8–34	103(a)	Kim, Rajan, Wyman[4]
1–14, 16–19, 29–34	103(a)	Riho, Rajan
1–34	103(a)	Riho, Rajan, Riho2[5]

[1] US 2011/0103156 A1, published May 5, 2011 (Ex. 1014).
[2] US 8,041,881 B2, issued Oct. 18, 2011 (Ex. 1015).
[3] US 2011/0026293 A1, published Feb. 3, 2011 (Ex. 1016).
[4] US 7,969,192 B2, issued June 28, 2011 (Ex. 1017).
[5] US 2010/0195364 A1, published Aug. 5, 2010 (Ex. 1018).

II. ANALYSIS

A. Discretionary Denial

1. Discretionary Denial Based on Fintiv

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 314(a) because the factors identified in *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv* Order"), weigh in favor of denying institution in view of the proceedings before the U.S. District Court for the Eastern District of Texas ("district court") in *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2-21-cv-00463 (E.D.Tex.) ("district court litigation"). Prelim. Resp. 50–56; Sur-reply 6. Petitioner argues we should not discretionarily deny institution. Pet. 144–45; Reply 6. For the reasons discussed below, we do not exercise discretion to deny institution.

Under § 314(a), the Director has discretion to deny institution of an *inter partes* review. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) ("[T]he PTO is permitted, but never compelled, to institute an IPR proceeding."); *see also* 37 C.F.R. § 42.4(a) ("The Board institutes the trial on behalf of the Director." In determining whether to exercise discretion to deny institution under 35 U.S.C. § 314(a), the Board considers whether the circumstances of a parallel district court proceeding are a basis for exercising such discretion. *Fintiv* Order 5–6.

A Memorandum from Director Vidal titled *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District*

Court Litigation (USPTO June 21, 2022) ("Interim Procedure")[6] sets forth the following:

> the PTAB will not deny institution of an IPR or PGR under *Fintiv* (i) when a petition presents compelling evidence of unpatentability; (ii) when a request for denial under *Fintiv* is based on a parallel ITC proceeding; or (iii) where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.

Interim Procedure 9.

Here, Petitioner has filed such a stipulation, which provides the following:

> Samsung stipulates that, if the Patent Trial and Appeal Board institutes an IPR proceeding for U.S. Patent No. 8,787,060 on the grounds presented in Samsung's petition in IPR2022-01428, Samsung will not pursue an invalidity defense in the Eastern District of Texas action (C.A. No. 21-463-JRG) that the patent claims subject to the instituted IPR are invalid based on grounds that were raised or reasonably could have been raised in the IPR.

Ex. 1051.

Thus, in light of Petitioner's stipulation, we do not exercise discretion to deny institution under 35 U.S.C. § 314(a).

2. Discretionary Denial Based on Claim Construction

Patent Owner argues that we should exercise discretion to deny if we disagree with the district court's constructions of "array die" or "chip select signal." Prelim. Resp. 49–51. We decline to discretionarily deny on this basis because Petitioner has demonstrated a reasonable likelihood of

[6] Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

prevailing on at least one claim under the district court's constructions, as explained below in section II.E.

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence.[7] *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

Citing the testimony of its declarant, Andrew Wolfe, Ph.D., Petitioner contends that a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field." Pet. 5 (citing Ex. 1003 ¶ 60). Petitioner also asserts that "[a]dditional training can substitute for educational or research experience, and vice versa," and Petitioner identifies particular technology with which a person of ordinary skill in the art would

[7] At this stage, Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims.

have been familiar, including JEDEC (Joint Electron Devices Engineering Council) industry standards and DRAM (dynamic random access memory) and SDRAM (synchronous DRAM) memory modules. Pet. 5.

Patent Owner does not dispute Petitioner's proposed skill level at this time. *See* Prelim. Resp. 20 ("For purposes of this preliminary response only, Patent Owner applies the skill level proposed by Petitioner.").

To the extent necessary, and for purposes of this Decision, we accept the uncontested assessment offered by Petitioner, with the exception of the qualifier "at least," which introduces vagueness as to the amount of experience.

D. Claim Construction

We interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)," and we must consider "[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a proceeding before the International Trade Commission, that is timely made of record." 37 C.F.R. § 42.100(b).

Petitioner contends that no express claim constructions are necessary. Pet. 21. Patent Owner argues that we should apply the district court's constructions for "array die" and "chip select signals." Prelim. Resp. 20–24. We provide a preliminary analysis of each of these terms below. The parties may address these and any other claim construction issues during the trial, and our final decision including any claim constructions will be based on the full record developed during the trial.

1. "Array Die"

The district court construed "array die" as "array die that is different from a DRAM circuit" based on an argument during prosecution of the '060

patent in which the applicant distinguished its "stacked array dies" from DRAM circuits 206A–D in U.S. Patent Application Publication 2008/0025137 A1 (Ex. 1011 ("Rajan137")). Ex. 2004, 31–32 (citing January 13, 2014 Amendment at 10); *see* Ex. 1002 ('060 prosecution history), 465 (January 13, 2014 Amendment at 10) ("Rajan does not disclose 'a plurality of stacked array dies.' Rajan merely stacks DRAM circuits 206A–D, which are different from array dies.").

Patent Owner argues that we should adopt the district court's construction so that there is a "consistent construction" between the two proceedings. Prelim. Resp. 22–23. Patent Owner, however, qualifies its position by arguing that "the statements it made during prosecution were specific to Rajan137's DRAM circuits 206A–D and this should be made clear to the jury through the order instead of having the expert explain it at trial." Prelim. Resp. 23 n.3 (citing Ex. 2005 (Patent Owner's objections to the district court claim construction order), 1–2); *see* Ex. 2005, 2 ("[T]he Court should make clear that the claimed array die is one that is 'different from Rajan's DRAM circuits 206A–D.'").

Although Patent Owner appears to walk this qualification back by arguing in its Sur-reply that it withdrew its objections to the district court claim construction (Sur-reply 1–2 (citing Exs. 2010, 2011)), Patent Owner's position here still appears to be that the term "array die" is one that is different from DRAM circuits 206A–D of Rajan137. For example, in disputing Petitioner's unpatentability contentions, Patent Owner argues that "the Petition contains no analysis on how or why Kim's or Riho's memory dies are different from Rajan137's DRAM circuits." Prelim. Resp. 25; *see also* Prelim. Resp. 26 ("Missing from the Petition is any analysis on why the referenced DRAM dies in the asserted grounds differ from Rajan137's

(EX1011's) 'DRAM circuits' 206A–D, an analysis that is required under the construction that Petitioner advocated and won in the District Court."). Further, in a district court pleading that Patent Owner cites (Sur-reply 2 (citing Ex. 2008)), Patent Owner argues that "Samsung fails to point to any evidence that its 'DRAM core dies' are or include the 'structural' 'DRAM circuits' of Rajan." Ex. 2008, 3.

Thus, Patent Owner appears to argue that the district court's construction is that the claimed array dies are different from Rajan137's DRAM circuits 206A–D, not all DRAM circuits.

For the reasons explained below in section II.E.3.a, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing under the district court's construction and also under that construction as interpreted by Patent Owner. Because the constructions advocated by Patent Owner do not impact the decision whether to institute, we need not resolve this claim construction issue at this time. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

2. "Chip Select Signals," "Chip Select Conduits"

Claims 6, 11–14, 16–19, and 29–34 recite "chip select signals" or "chip select conduits." Patent Owner argues that the district court construed the term "chip select signals" and associated "chip select conduits" to "exclude[] situations in which a chip select signal could enable multiple array dies at once" and contends that we should adopt this construction. Prelim. Resp. 23–24 (citing Ex. 2004, 33–34). For the reasons explained below in section II.E.6, we determine that Petitioner has demonstrated a

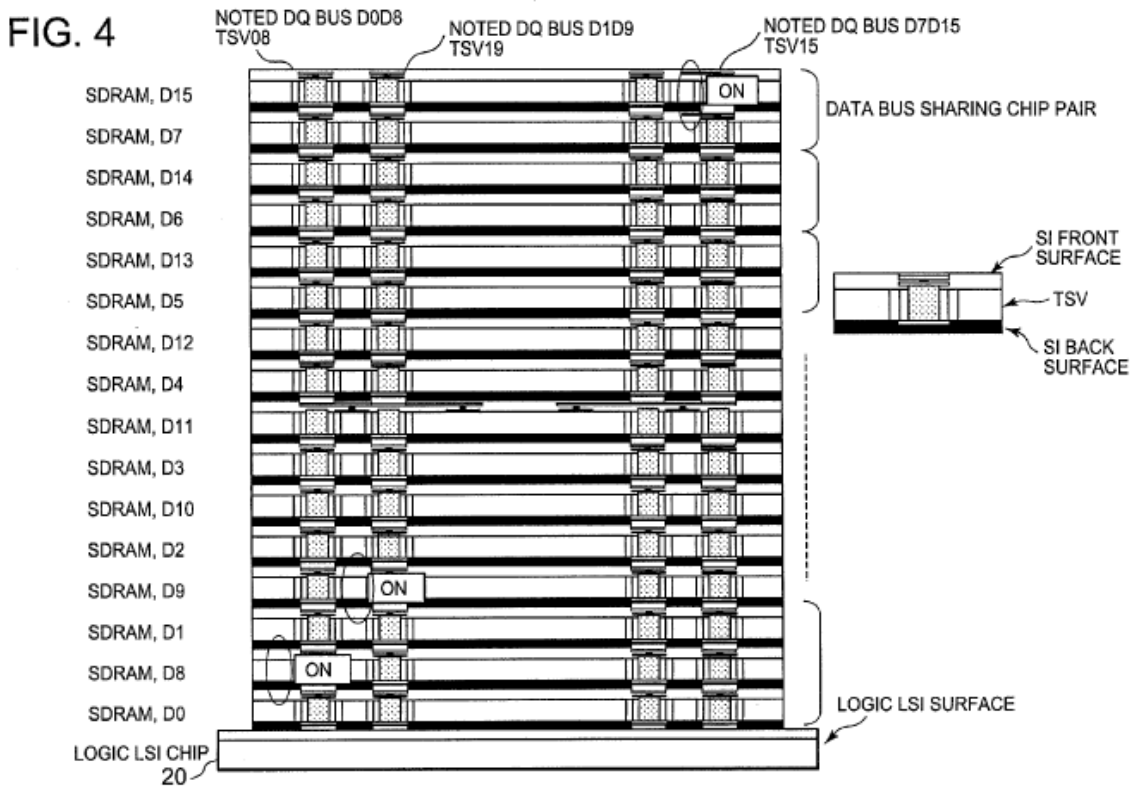
reasonable likelihood of prevailing under the district court's construction, and, therefore, we need not further address this claim construction at this time.

E. Alleged Obviousness over Riho and Rajan (Claims 1–14, 16–19, 29–34)

We begin our analysis with Petitioner's fourth listed ground in which Petitioner asserts that claims 1–14, 16–19, and 29–34 are unpatentable as obvious over the combined teachings of Riho and Rajan. Pet. 3, 91–138.

1. Overview of the Prior Art

Riho discloses a memory chip configuration in which memory chips are stacked on a logic chip, such as shown in Figure 4 below.



Riho's Figure 4 above shows SDRAM chips D0–D15 stacked on LSI logic chip 20 in the following order: D0, D8, D1, D9, D2, D10, D3, D11, D4, D12, D5, D13, D6, D14, D7, D15. Ex. 1016 ¶ 62. SDRAMs D0–D7 form a

first group, and SDRAMs D8–D15 form a second group. Ex. 1016 ¶ 62. The adjacent two SDRAMs from each group form a pair, such that D0 and D8 form a pair, D1 and D9 form a pair, and D7 and D15 form a pair. Ex. 1016 ¶ 62. Riho explains that each pair shares a data signal via a through-silicon via (TSV), such that, as illustrated in Figure 4, D0 and D8 share TSV08, D1 and D9 share TSV19, and D7 and D15 share TSV715.[8] Ex. 1016 ¶¶ 62–63. Riho explains that sharing TSVs reduces the load on each SDRAM chip. Ex. 1016 ¶ 103.

Rajan discloses using an interface circuit to emulate characteristics of particular memory even though the physical memory may not have those characteristics, which allows the "use of low cost memory chips in manufacturing high capacity memory modules." Ex. 1015, 1:51–54, 3:24–43. Rajan explains that the interface circuit may comply with JEDEC standards. Ex. 1015, 4:20–24.

2. Overview of Petitioner's Contentions for Claim 1

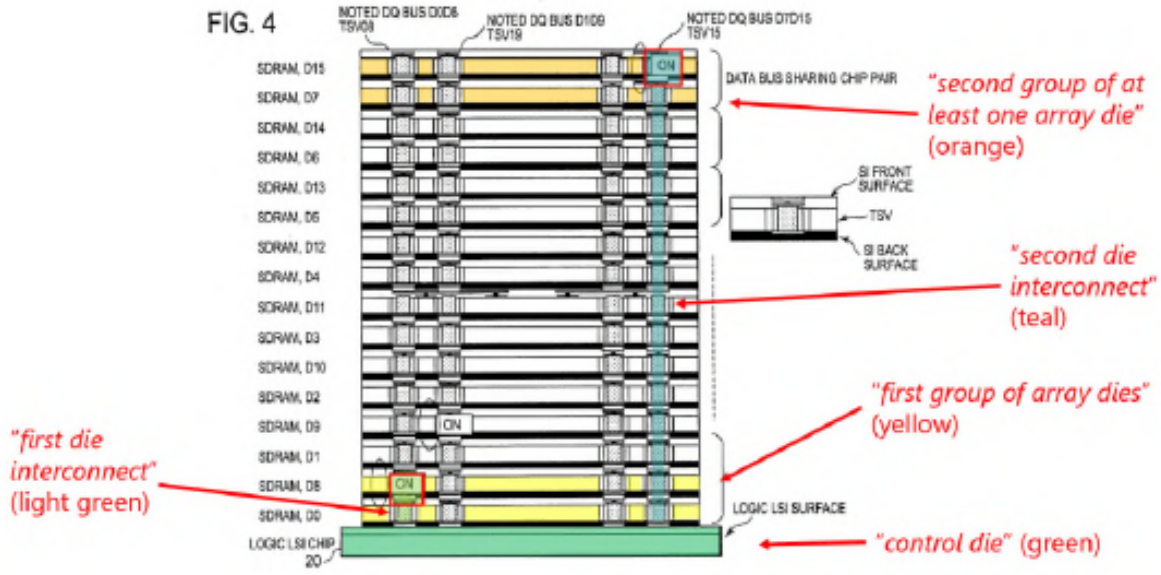
Petitioner argues that Riho discloses a memory package (preamble) having input/output terminals (1.b). Pet. 94–98 (citing Ex. 1016 ¶¶ 26, 30–31, Figs. 1, 2; Ex. 1003 ¶¶ 706–718); *see* Ex. 1016 ¶ 26 (describing, with reference to Figure 1, "external terminals (not illustrated) . . . disposed on the lower side of the logic LSI chip 20"). Petitioner argues that it would have been obvious "to implement Riho's memory package with Rajan's terminals . . . to comply with the JEDEC standards" based on "Rajan's suggestion to implement address, control and data terminals according to JEDEC standards" and because "JEDEC standards were influential and

[8] Although Figure 4 labels this "TSV15," Riho's written description refers to this as "TSV715." Ex. 1016 ¶¶ 63, 65.

well-known." Pet. 93, 96–98 (citing Ex. 1003 ¶¶ 683–692, 715–716; Ex. 1015, 2:6–7, 3:52–54, 4:20–24, 5:36–43, 6:30–7:67, 8:8–11, Figs. 4, 18).[9]

For element 1.c ("a plurality of stacked array dies including a first group of array dies and a second group of at least one array die, each array die having data ports"), Petitioner identifies Riho's SDRAM chips D0–D15 as examples of stacked chips each having a die and identifies SDRAMs D0 and D8 as a first group of array dies and SDRAMs D7 and D15 as a second group of array dies. Pet. 98–99 (citing Ex. 1016 ¶¶ 27, 29, 45–47, 49, 62, Figs. 1, 2; Ex. 1003 ¶¶ 719–726; Ex. 1018, code (57), Fig. 1).

For elements 1.d.1 and 1.d.2, Petitioner provides the annotated version of Figure 4 below.

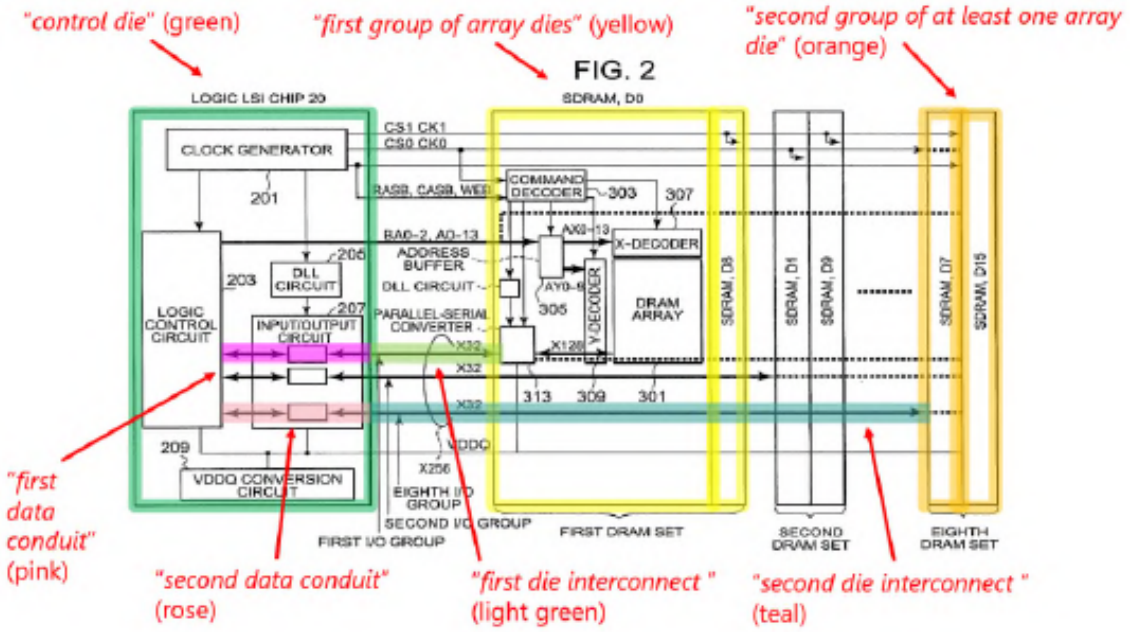


Pet. 101. In the annotated version of Figure 4 above, Petitioner identifies TSV08 as the "first die interconnect" in light green and TSV715 as the "second die interconnect" in teal. Pet. 100–01. Petitioner argues that

[9] Throughout this Decision, we omit the underline emphasis Petitioner provided for the names of the prior art references.

TSV08 is in electrical communication with D0 and D8 ("first group") but not with D7 and D15 ("second group") and that TSV715 is in electrical communication with D7 and D15 but not with D0 and D8. Pet. 100–01 (citing Ex. 1016 ¶¶ 45–46, 64–65, Figs. 2, 4; Ex. 1003 ¶¶ 727–744). Petitioner argues that "Rajan also teaches this arrangement to reduce load." Pet. 101 (citing Ex. 1015, 5:36–43, 5:63–6:2, Fig. 4; Ex. 1003 ¶¶ 739–743).

For element 1.e.1 ("control die"), Petitioner identifies Riho's logic LSI chip 20. Pet. 102–103 (citing Ex. 1016 ¶ 26, Fig. 1; Ex. 1003 ¶¶ 745–752). Petitioner provides the annotated version of Riho's Figure 2 below to illustrate the first and second data conduits of elements 1.e.2 and 1.e.3.



Pet. 104. Riho's Figure 2 shows logic LSI chip 20 and SDRAM D0 in detail with constituent components and shows other SDRAMs simply as rectangles. Referring to the annotated version of Riho's Figure 2 above, Petitioner argues that the lines colored pink are a "first data conduit" between input/output terminals and the "first die interconnect" (light green) and that the lines colored rose are a "second data conduit" between the data

terminal and the "second die interconnect" (teal). Pet. 103–04 (citing Ex. 1016 ¶¶ 26, 39–40, 45–46, Fig. 2; Ex. 1003 ¶¶ 756–762); *see also* Pet. 104–05 (discussing external data terminals for JEDEC-compliant devices).

For element 1.e.4 (including "control circuit"), Petitioner argues that Riho's logic control circuit 203 and input/output circuit 207 control states of the first and second data conduits by "communicating data in the read or write direction with the correct timing." Pet. 106–07 (citing Ex. 1016 ¶¶ 39–40, 45, 53, Fig. 2; Ex. 1003 ¶¶ 770–778). Petitioner further argues that a person of ordinary skill in the art "would have been motivated to look to Rajan for details about how Riho's control chip can interface with a host system, and Rajan discloses external terminals for control signals to read/write data according to the timing requirements in the JEDEC standards." Pet. 107–08 (citing Ex. 1003 ¶¶ 773–774; Ex. 1015, 11:12–12:13, Fig. 14).

3. Patent Owner's Arguments and Our Preliminary Analysis

Patent Owner makes two arguments against Petitioner's challenge to claim 1 based on the combination of Riho and Rajan, which we address below.

a) Element 1.c ("array dies")

Patent Owner disputes Petitioner's showing for element 1.c's "array dies." Prelim. Resp. 25–30. According to Patent Owner, "the Petition contains no analysis on how or why . . . Riho's memory dies are different from Rajan137's DRAM circuits, an interpretation that it advocated and persuaded the District Court to adopt." Prelim. Resp. 25. On this record, however, we see nothing to indicate that Riho's SDRAM chips D0–D15 are the same as Rajan137's DRAM circuits. We note at least one difference is

that Riho discloses that each of D0–D15 is a 2 Gbit memory (Ex. 1016 ¶¶ 35, 47), whereas Rajan137 states that "the stack of DRAM circuits 206A-D may include eight 512 Mb DRAM circuits . . . to resemble a single 4 Gb DRAM circuit" (Ex. 1011 ¶ 45).

Furthermore, to the extent the claim excludes any DRAM chips at all, Riho explains that its disclosures are not limited to SDRAM. Ex. 1016 ¶ 135; *see* Reply 4. Patent Owner counters that Petitioner "relies on DRAM-based 'JEDEC standards' and textbooks . . . and compliance thereof to argue that the limitations are met." Sur-reply 3. Petitioner's contention, however, is that it would have been obvious "to create a package with an *interface* that complied with the well-known JEDEC standards." Pet. 93 (emphasis added); *see also* Pet. 94 ("Such a combination would have been well within a [person of ordinary skill in the art]'s level of skill since *emulating* a standard JEDEC interface was well-known, as demonstrated by Rajan . . . and the 060 Patent's admitted prior art . . . ." (emphasis added)). Thus, on this record, we do not agree with Patent Owner that Petitioner's reliance on JEDEC compliance undermines Petitioner's contentions.

For the reasons given by Petitioner and those discussed above, we are sufficiently persuaded that Riho teaches the subject matter of element 1.c applying the district court's construction of "array die" and applying Patent Owner's interpretation of the district court's construction.

b) Elements 1.d.1 and 1.d.2 ("not in electrical communication")

Second, Patent Owner argues that Petitioner's contentions fail for elements 1.d.1 and 1.d.2 because each of the TSVs ("die interconnect[s]") is electrically connected to a switch circuit on each die such that Riho does not teach die interconnects that are "not in electrical communication" with certain array dies as recited in claim 1. Prelim. Resp. 36–37 (citing Ex. 1016

¶ 45, Figs. 4–6). Patent Owner argues that there is no data exchange with certain chips because the switches on those chips are turned off, not because the TSVs have no electrical connection to the chips. Prelim. Resp. 37–38 (citing Ex. 1016 ¶¶ 72–75, 91, Fig. 5). Patent Owner further argues that "Petitioner does not explain . . . how Riho's structure differs from a conventional multi-drop architecture" as allegedly disclosed in the prior art configuration of Figure 1A of the '060 patent. Prelim. Resp. 39.

On the present record, we find Petitioner's contentions sufficiently persuasive. Riho describes the TSV configuration as follows: "[T]he data signal DQ TSV19 and circuits formed at the front surfaces of the SDRAMs D1 and D9 are in a conductive state (i.e. on state) while the data signal DQ TSV19 is *not electrically connected to the SDRAMs other than the SDRAMs D1 and D9*." Ex. 1016 ¶ 65 (emphasis added); *see* Pet. 100–01 (citing this disclosure). Thus, Riho expressly discloses that there is no electrical connection to SDRAMs other than the pair with which the TSV is in a "conductive state." On this record, we disagree with Patent Owner's argument that Riho's use of a switch to accomplish this is no different from the prior art configuration in Figure 1A of the '060 patent. *See* Prelim. Resp. 39. In describing the state of the prior art, the '060 patent explains that "a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die interconnects *and the corresponding circuitry of the array dies*," which requires a driver "large enough to overcome the load on the driver." Ex. 1001, 2:8–13 (emphasis added). Riho does not present the same issue because the TSVs are "not electrically connected to" all of the SDRAMs, as explained in paragraph 65 of Riho, thus obviating the need for drivers large enough to drive signals to all of the circuitry on all chips.

Patent Owner states that Petitioner "argued in the District Court that a TSV is in electrical communication with an SDRAM die even if the driver/receiver circuit for the associated memory arrays on the die is turned off." Prelim. Resp. 38. Patent Owner, however, does not cite any support for this assertion. In its Sur-reply, Patent Owner cites an email allegedly showing that Petitioner regards Riho as a non-infringing alternative. Sur-reply 4 (citing Ex. 2012). On this record, however, we do not view this position as inconsistent with Petitioner's contentions in this proceeding, which are based on obviousness, not anticipation. *Cf. Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1378 (Fed. Cir. 2001) ("[I]t is axiomatic that that which would literally infringe if later anticipates if earlier.").

For the reasons given by Petitioner and those discussed above, we are sufficiently persuaded that Riho teaches die interconnects that are "not in electrical communication" with certain array dies and that the asserted combination renders obvious the subject matter of elements 1.d.1 and 1.d.2.

4. Preliminary Determination for Claim 1

For the reasons discussed above and based on Petitioner's contentions and evidence, summarized above, we are persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claim 1 is unpatentable as obvious over the combined teachings of Riho and Rajan.

5. Claims 2–5 and 7–10

Petitioner asserts that dependent claims 2–5 and 7–10 are unpatentable as obvious over the combined teachings of Riho and Rajan. Pet. 108–16, 119–27. Patent Owner relies on the arguments addressed above in § II.E.3 for claims 2–5 and 7–10 and does not set forth additional

arguments for these claims at this stage of the proceeding. We have reviewed Petitioner's contentions, and we are sufficiently persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claims 2–5 and 7–10 are unpatentable as obvious over the combined teachings of Riho and Rajan.

6. Claims 6, 11–14, 16–19, 29–34

Petitioner asserts that claims 6, 11–14, 16–19, and 29–34 are unpatentable as obvious over the combined teachings of Riho and Rajan. Pet. 116–19, 127–38. For these claims, we focus on the disputed issue between the parties, which is whether the asserted prior art teaches "chip select signals" or "chip select conduits" as recited in these claims. Prelim. Resp. 47–49.

Claim 6 depends from claim 1 and recites that "the control die further comprises chip-select conduits" and that "the memory package further compris[es] third die interconnects coupled between respective chip select conduits and respective ones of the plurality of stacked array dies." Independent claim 11 recites "chip select conduits for providing chip select signals to respective array dies."

Petitioner argues that Riho teaches signals that select the SDRAM chips, including chip selection signals CS0CK0 and CS1CK1 and command signals such as bank address signals BA0–2. Pet. 116–19 (citing Ex. 1016 ¶¶ 33, 38, Fig. 2; Ex. 1003 ¶¶ 818–832). Petitioner asserts that the "060 Patent also admits that transmitting separate chip-select signals through '*die interconnects*' to select an '*array die*' was well-known at the time." Pet. 118 (citing Ex. 1001, 1:49–56, Figs. 1A, 1B; Ex. 1003 ¶ 830).

Patent Owner argues that Riho has only two chip select signals, CS0CK0 and CS1CK1, each of which selects multiple dies, and, therefore,

that Petitioner's contentions fail to meet the district court's constructions for "chip select signal" and "chip select conduit." Prelim. Resp. 47–48 (citing Ex. 1016 ¶ 37, Fig. 2). This argument, however, does not address Petitioner's contentions that Riho discloses additional signals sent to select particular dies, such as bank address signals BA0–2, and that it would have been obvious to "transmit[] separate chip-select signals through 'die interconnects' to select an 'array die.'" Pet. 116–18 (emphasis omitted). On this record, we are sufficiently persuaded that using separate chip select signals for each die was a known option for a person of ordinary skill in the art. *See* Ex. 1003 ¶ 830 (Dr. Wolfe's testimony that transmitting separate chip select signals was well known); *see also* Ex. 1015, 6:34–38 (Rajan's disclosure that "extra address bits may be decoded by the buffer chip to individually select the DRAM chips, utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack"), *cited in* Pet. 61.

For the reasons given by Petitioner and those discussed above, we are sufficiently persuaded that it would have been obvious, based on the combination of Riho and Rajan, for separate chip selection signals to be used for each array die.

We are sufficiently persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claims 6, 11–14, 16–19, and 29–34 are unpatentable as obvious over the combined teachings of Riho and Rajan.

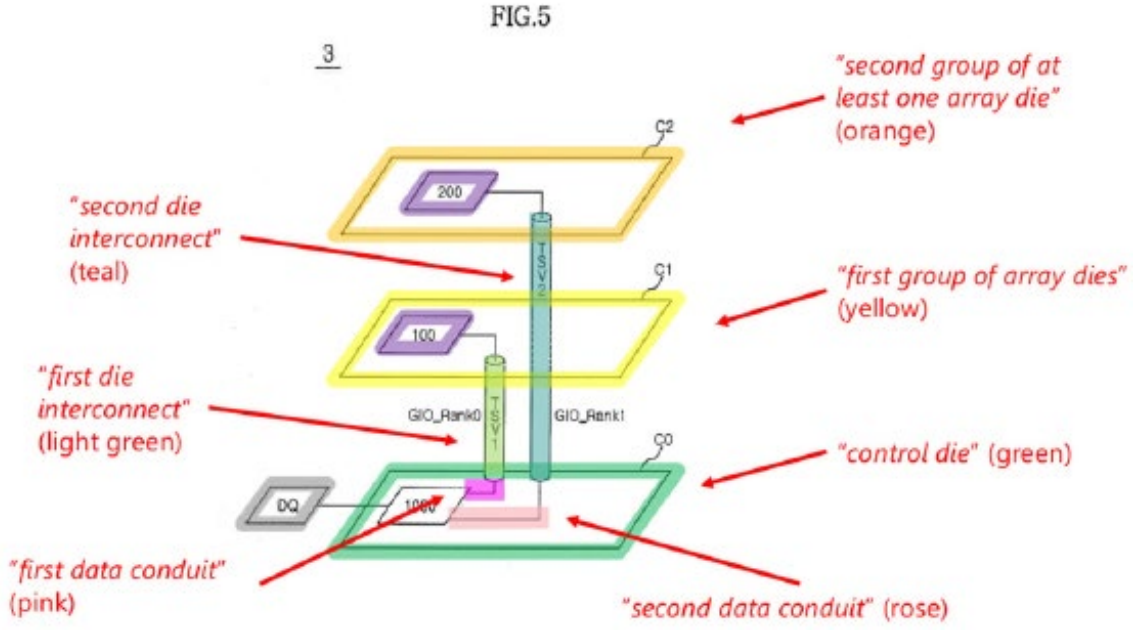
F. Alleged Obviousness over Kim and Rajan (Claims 1–6, 8–14, 16–19, 29–34)

Petitioner asserts that claims 1–6, 8–14, 16–19, and 29–34 are unpatentable as obvious over the combined teachings of Kim and Rajan. Pet. 3, 21–81. Having determined that the Petition meets the threshold for

institution (reasonable likelihood of prevailing as to at least one of the challenged claims) based on the combination of Riho and Rajan, the remainder of this Decision focuses on the parties' disputes to provide guidance to the parties for the trial.

1. Overview of Petitioner's Contentions for Claim 1

To illustrate its contentions based on Kim, Petitioner provides the following annotated version of Kim's Figure 5:



Pet. 41. Kim's Figure 5 depicts main chip C0 with TSVs connecting C0 to each of stacked memory chips C1 and C2. Ex. 1014 ¶ 48. In the annotated figure above, Petitioner maps depicted components to elements of claim 1 as follows: chip C1 (yellow) as "first group of array dies"; chip C2 (orange) as "second ground of at least one array die"; chip C0 (green) as "control die"; TSV1 (light green) from C0 to C1 as "first die interconnect"; TSV2 (teal) from C0 to C2 as "second die interconnect"; box labeled "DQ" (gray) as "input/output terminals"; line (pink) from data input/output section 1000 to

TSV1 as "first data conduit"; and line (rose) from data input/output section 1000 to TSV2 as "second data conduit." Pet. 30–47.

Petitioner argues that a person of ordinary skill in the art would have been motivated to make Kim's memory package compatible with JEDEC standards based on Rajan's teachings. Pet. 24–27. Petitioner also argues that a person of ordinary skill in the art would have been motivated to have multiple memory chips share a TSV because this was a known option and "would not require creating new TSVs (which would add space and circuitry) and would allow emulating the JEDEC standard required by external devices." Pet. 28–29.

2. Patent Owner's Arguments for Claim 1

a) Element 1.c ("array dies")

As to element 1.c regarding the recited "array dies," Patent Owner argues that Petitioner has not shown that Kim's or Rajan's memory dies are different from Rajan137's DRAM circuits, which Patent Owner asserts are excluded from the scope of the claim. Prelim. Resp. 20–22, 25–30. On this record, we disagree. As Petitioner correctly points out, Kim does not even mention DRAM and thus is not limited to DRAM. *See* Reply 3. Furthermore, as Petitioner points out (Reply 2–3), Rajan states that "any type of memory whatsoever" may be used in its disclosure and lists non-DRAM memories. Ex. 1015, 15:3–9. Patent Owner argues that Rajan137 also states that its disclosure applies to memory types other than DRAM, which, according to Patent Owner, shows that Rajan and Rajan137 are the same in this respect. Sur-reply 2–3 (citing Ex. 1011 ¶¶ 18, 43). But the arguments during prosecution of the '060 patent specifically cited Rajan137's "DRAM circuits 206A–D," not other types of memory. Ex. 1002, 465. Therefore, to the extent there was disclaimer of subject

matter during prosecution (*see* Prelim. Resp. 11–14, 20–23), it would appear to be disclaimer of Rajan137's "DRAM circuits 206A–D," not a disclaimer of all memory chips.

Patent Owner also argues that Petitioner "relies on DRAM-based 'JEDEC standards' and textbooks . . . and compliance thereof to argue that the limitations are met." Sur-reply 3. But as discussed above in section II.E.3.a for a similar argument as to Riho, Petitioner's contention is that it would have been obvious "to create a package with an *interface* that complied with the well-known JEDEC standards." Pet. 93 (emphasis added); *see also* Pet. 94 (asserting that "emulating a standard JEDEC interface was well-known"). Thus, on this record, we do not agree with Patent Owner that Petitioner's reliance on JEDEC compliance undermines Petitioner's contentions.

On this record, we are sufficiently persuaded by Petitioner's contentions that the combination of Kim and Rajan teaches "array dies" that are "different from a DRAM circuit," as in the district court's construction, and also that are different from Rajan137's DRAM circuits 206A–D, as in Patent Owner's interpretation of the district court's construction.

b) Operability of modified Kim

Patent Owner also argues that Petitioner has not shown how including additional dies connected to the same TSV in Kim would result in an operable device and that there is "no competent evidence" to support the operability of the combination. Prelim. Resp. 30–36 (emphasis omitted). On this record, we disagree. As Petitioner points out (Pet. 37), Kim discloses that "any number of" memory chips may be used and that "a person having ordinary skill in the art will appreciate that the technical concept of the present invention can be applied to a semiconductor memory

apparatus . . . divided into three or more ranks." Ex. 1014 ¶¶ 48, 50. In support of its contentions, Petitioner points to Rajan's disclosure of multiple stacked memory chips connected to the same data bus. Pet. 38–39 (citing Ex. 1015, Fig. 4; Ex. 1003 ¶¶ 206–212). Petitioner also cites another reference that Petitioner asserts "show[s] multiple groups of stacked dies, where each die in a group is connected to the same data interconnect." Pet. 37–38 (citing US 7,796,446 B2, filed Sept. 19, 2008 (Ex. 1024, "Ruckerbauer"), 9:14–18, Fig. 5). Ruckerbauer discloses a memory stack in which two memory dies are connected to data transfer path 12a and three memory dies are connected to data transfer path 12b. Ex. 1024, 9:4–18, Fig. 5. Patent Owner cites Ruckerbauer's disclosure of "internal signal paths" and argues that "dies belonging to the same rank each have a different signaling pathway." Prelim. Resp. 34 (citing Ex. 1024, 10:60–62, 10:64–67). On this record, we do not see that this disclosure undermines Ruckerbauer's express disclosure of multiple memory dies sharing one transfer data path, discussed above.

Based on the foregoing, we are sufficiently persuaded by Petitioner's evidence that it would have been within the knowledge and skill of a person of ordinary skill in the art to connect multiple memory chips to Kim's TSVs in a manner that is operable. *See* Ex. 1003 ¶¶ 219–227.

3. Claims 6, 11–14, 16–19, 29–34

Similar to its arguments for the Riho ground discussed above in section II.E.6, Petitioner argues that Rajan teaches using separate chip select signals for each memory chip in a stack and that JEDEC requires this. Pet. 59–62 (citing, *inter alia*, Ex. 1015, 6:34–38). Patent Owner argues that Petitioner's contentions for claims reciting "chip select signal" or "chip select conduit" fail because the chip select signal in the proposed

combination would select more than one chip, contrary to the district court's construction. Prelim. Resp. 42–46. More particularly, Patent Owner argues that, "according to Petitioner's own evidence, a JEDEC-compliant chip select signal that it claims a [person of ordinary skill in the art] would have installed in modified Kim would select an entire rank of DRAM devices," i.e., multiple DRAM devices. Prelim. Resp. 46. Petitioner argues that its position is that "***each*** die in the group is in a ***separate*** rank and receives a ***separate*** 'chip select signal,'" consistent with the Petition's discussion of both JEDEC and Rajan disclosing separate chip select signals for each chip in a stack. Reply 5–6 (citing Pet. 61–62). Patent Owner counters that "the Reply does not explain where in the Petition it argues that each die in the modified Kim (where a TSV is connected to more than one die) belongs to a separate rank or receives a separate chip select signal." Sur-reply 5.

On this record, we disagree with Patent Owner's argument because Petitioner relies on Rajan's disclosure of "utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack" (Ex. 1015, 6:34–38). Pet. 61 (citing Ex. 1003 ¶¶ 329–330). Thus, we disagree with Patent Owner's contention that Petitioner has not shown "where in the Petition it argues that each die in the modified Kim (where a TSV is connected to more than one die) belongs to a separate rank or *receives a separate chip select signal*." *See* Sur-reply 5 (emphasis added). Furthermore, to the extent Patent Owner is correct that a JEDEC-compliant chip select signal selects multiple chips and thus does not meet the language of the claims, Petitioner's reliance on the JEDEC standard may, on its own, be insufficient to show obviousness.

4. Preliminary Determination for Claims 1–6, 8–14, 16–19, 29–34

We have reviewed Petitioner's contentions based on the combination of Kim and Rajan and find them sufficiently persuasive on this record.

G. Remaining Grounds

As noted above in § I.E, Petitioner asserts the following additional grounds: obviousness of claims 1–14, 16–19, and 29–34 over the combined teachings of Kim, Rajan, and Riho; obviousness of claims 1–6 and 8–34 over the combined teachings of Kim, Rajan, Wyman; and obviousness of claims 1–34 over the combined teachings of Riho, Rajan, and Riho2. Pet. 3. At this stage of the proceeding, Patent Owner does not separately address Petitioner's contentions in these grounds. We have reviewed Petitioner's contentions, and we determine, on this record, that Petitioner has shown a reasonable likelihood of prevailing on these grounds.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging at least one claim of the '060 patent, and we institute *inter partes* review of all challenged claims on all grounds raised in the Petition. *See* 37 C.F.R. 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."). At this stage of the proceeding, we have not made a final determination with respect to the patentability of any of the challenged claims or the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted as to claims 1–34 of the '060 patent on all challenges raised in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which will commence on the entry date of this decision.

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Paper 13
Date: April 12, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-01427
Patent 9,318,160 B2

Before PATRICK M. BOUCHER, DANIEL J. GALLIGAN, and SHEILA F. McSHANE, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Samsung Electronics Co., Ltd. ("Petitioner") filed a petition for *inter partes* review (Paper 1 ("Pet." or "Petition")) challenging claims 1–20 of U.S. Patent 9,318,160 B2 (Ex. 1001 ("'160 patent")). Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). With our authorization, Petitioner filed a Reply to Patent Owner's Preliminary Response (Paper 9 ("Reply")), and Patent Owner filed a Sur-reply to Petitioner's Preliminary Reply (Paper 10 ("Sur-reply")).

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute review. The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless the information presented in the Petition and the Preliminary Response shows "there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition."

For the reasons explained below, we institute an *inter partes* review of all challenged claims on all grounds raised in the Petition.

B. Related Matters

As required by 37 C.F.R. § 42.8(b)(2), the parties identify various related matters, including IPR2022-01428, which involves related Patent 8,787,060 B2 ("'060 patent"). Pet. 1; Paper 3 at 1; *see also* Ex. 1001, code (63) (identifying the '160 patent as a continuation of the '060 patent).

C. Real Parties in Interest

Petitioner identifies itself and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 1. Patent Owner identifies itself as the real party in interest. Paper 3 at 1.

D. The '160 Patent and Illustrative Claim

The '160 patent relates to computer memory devices and, more specifically, to reducing the load of drivers in memory. Ex. 1001, 1:20–24. As background, the '160 patent describes an existing memory package with reference to Figure 1A, reproduced at right, which shows memory package 100 with control die 130 and three array dies 110. Ex. 1001, 1:32–46. Control die 130 has driver 134, which drives data signals from control die 130 to each array die via interconnect 142, and driver 140, which drives command and address signals to each array die. Ex. 1001, 1:37–44. The '160 patent explains that "a load exists on each of the drivers 134, 140 . . . by virtue of the drivers being in electrical communication with the corresponding die interconnects and the corresponding circuitry of the array dies." Ex. 1001, 2:10–13. The '160 patent discloses that, "to drive a signal along a die interconnect, a driver typically must be large enough to overcome the load on the driver" and that "a larger driver not only consumes more space on the control die, but also consumes more power." Ex. 1001, 2:13–17.

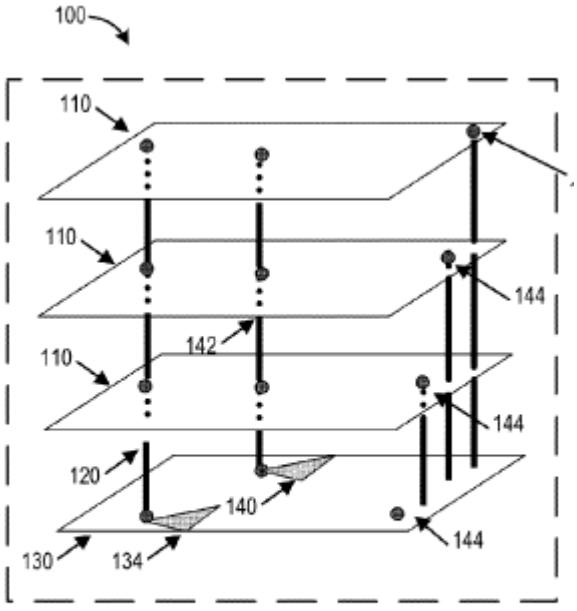


FIG. 1A

The '160 patent proposes that driver size and power consumption can be reduced "by increasing the number of die interconnects and reducing the number of array dies that are in electrical communication with each die

interconnect." Ex. 1001, 4:25–29. The '160 patent illustrates an exemplary configuration in Figure 2, reproduced at right, which shows memory package 200 with control die 230 and four array dies 210a–210d. Ex. 1001, 5:15–16. Control die 230 is connected to array dies 210a and 210b by die interconnect 220a, as shown by the darkened circles. Ex. 1001, 5:66–6:4. Die interconnect 220b connects control die 230 to array dies 210c and 210d, as shown by the darkened circles, but die interconnect 220b is not electrically connected to array dies 210a and 210b, as shown by the unfilled circles. Ex. 1001, 6:12–26. Thus, in the disclosure of Figure 2, the die interconnects do not connect to each array die as in Figure 1A discussed above.

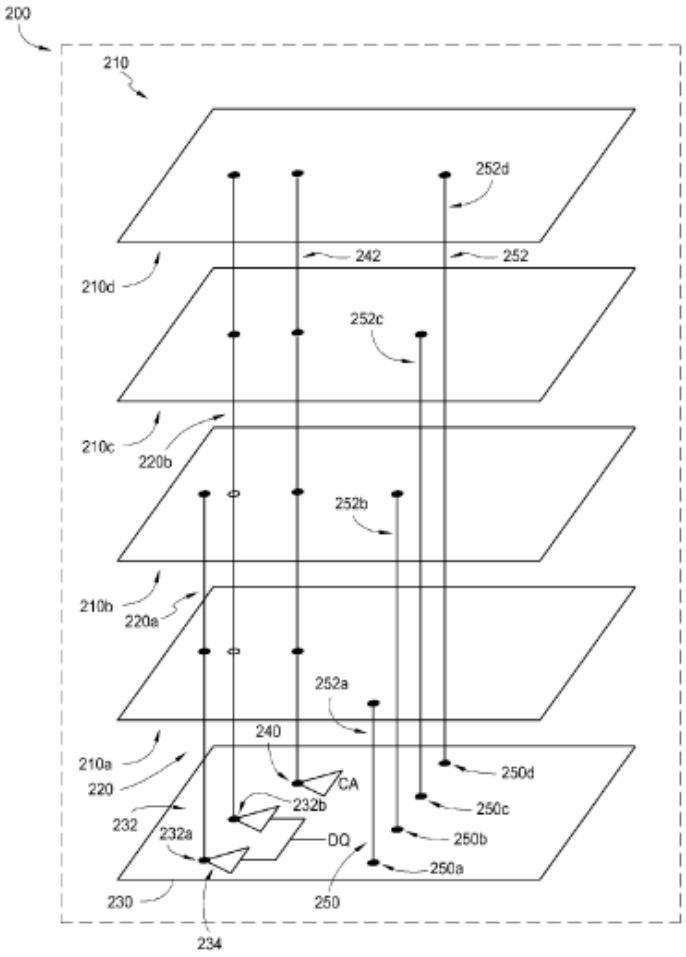


FIG. 2

Claim 1 is illustrative and is reproduced below with Petitioner's claim element identifiers in brackets.

1. [1.a] A memory package, comprising:

   [1.b] data terminals and control terminals;

   [1.c] stacked array dies including a first group of array dies and a second group of at least one array die;

> [1.d.1] first die interconnects and second die interconnects, the first die interconnects in electrical communication with the first group of array dies and not in electrical communication with the second group of at least one array die, [1.d.2] the second die interconnects in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and
>
> [1.e.1] a control die comprising [1.e.2] first data conduits between the first die interconnects and the data terminals, and [1.e.3] second data conduits between the second die interconnects and the data terminals, [1.e.4] the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, [1.e.5] the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.

E. Asserted Grounds of Unpatentability

Petitioner presents the following grounds (Pet. 3):

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1–20	103(a)	Kim,[1] Rajan,[2] Wyman[3]
1–20	103(a)	Riho,[4] Rajan, Riho2[5]

[1] US 2011/0103156 A1, published May 5, 2011 (Ex. 1014).
[2] US 8,041,881 B2, issued Oct. 18, 2011 (Ex. 1015).
[3] US 7,969,192 B2, issued June 28, 2011 (Ex. 1017).
[4] US 2011/0026293 A1, published Feb. 3, 2011 (Ex. 1016).
[5] US 2010/0195364 A1, published Aug. 5, 2010 (Ex. 1018).

II. ANALYSIS

A. Discretionary Denial

1. Discretionary Denial Based on Fintiv

Patent Owner argues that we should exercise discretion to deny institution under 35 U.S.C. § 314(a) because the factors identified in *Apple, Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (precedential) ("*Fintiv* Order"), weigh in favor of denying institution in view of the proceedings before the U.S. District Court for the Eastern District of Texas ("district court") in *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 2-21-cv-00463 (E.D.Tex.) ("district court litigation"). Prelim. Resp. 52–57; Sur-reply 6. Petitioner argues we should not discretionarily deny institution. Pet. 128–29; Reply 6. For the reasons discussed below, we do not exercise discretion to deny institution.

Under § 314(a), the Director has discretion to deny institution of an *inter partes* review. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) ("[T]he PTO is permitted, but never compelled, to institute an IPR proceeding."); *see also* 37 C.F.R. § 42.4(a) ("The Board institutes the trial on behalf of the Director." In determining whether to exercise discretion to deny institution under 35 U.S.C. § 314(a), the Board considers whether the circumstances of a parallel district court proceeding are a basis for exercising such discretion. *Fintiv* Order 5–6.

A Memorandum from Director Vidal titled *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District*

Court Litigation (USPTO June 21, 2022) ("Interim Procedure")[6] sets forth the following:

> the PTAB will not deny institution of an IPR or PGR under *Fintiv* (i) when a petition presents compelling evidence of unpatentability; (ii) when a request for denial under *Fintiv* is based on a parallel ITC proceeding; or (iii) where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.

Interim Procedure 9.

Here, Petitioner has filed such a stipulation, which provides the following:

> Samsung stipulates that, if the Patent Trial and Appeal Board institutes an IPR proceeding for U.S. Patent No. 9,318,160 on the grounds presented in Samsung's petition in IPR2022-01427, Samsung will not pursue an invalidity defense in the Eastern District of Texas action (C.A. No. 21-463-JRG) that the patent claims subject to the instituted IPR are invalid based on grounds that were raised or reasonably could have been raised in the IPR.

Ex. 1051.

Thus, in light of Petitioner's stipulation, we do not exercise discretion to deny institution under 35 U.S.C. § 314(a).

2. Discretionary Denial Based on Claim Construction

Patent Owner argues that we should exercise discretion to deny if we disagree with the district court's constructions of "array die" or "chip select signal." Prelim. Resp. 50–51. We decline to discretionarily deny on this basis because Petitioner has demonstrated a reasonable likelihood of

[6] Available at https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

prevailing on at least one claim under the district court's constructions, as explained below in section II.E.

B. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any secondary considerations, if in evidence.[7] *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

Citing the testimony of its declarant, Andrew Wolfe, Ph.D., Petitioner contends that a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field." Pet. 5 (citing Ex. 1003 ¶ 60). Petitioner also asserts that "[a]dditional training can substitute for educational or research experience, and vice versa," and Petitioner identifies particular technology with which a person of ordinary skill in the art would

[7] At this stage, Patent Owner does not present any objective evidence of nonobviousness (i.e., secondary considerations) as to any of the challenged claims.

have been familiar, including JEDEC (Joint Electron Devices Engineering Council) industry standards and DRAM (dynamic random access memory) and SDRAM (synchronous DRAM) memory modules. Pet. 5.

Patent Owner does not dispute Petitioner's proposed skill level at this time. *See* Prelim. Resp. 21 ("For purposes of this preliminary response only, Patent Owner applies the skill level proposed by Petitioner.").

To the extent necessary, and for purposes of this Decision, we accept the uncontested assessment offered by Petitioner with the exception of the qualifier "at least," which introduces vagueness as to the amount of experience.

D. Claim Construction

We interpret claim terms using "the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)," and we must consider "[a]ny prior claim construction determination concerning a term of the claim in a civil action, or a proceeding before the International Trade Commission, that is timely made of record." 37 C.F.R. § 42.100(b).

Petitioner contends that no express claim constructions are necessary. Pet. 23. Patent Owner argues that we should apply the district court's constructions for "array die" and "chip select signals." Prelim. Resp. 21–25. We provide a preliminary analysis of each of these terms below. The parties may address these and any other claim construction issues during the trial, and our final decision including any claim constructions will be based on the full record developed during the trial.

1. "Array Die"

The district court construed "array die" as "array die that is different from a DRAM circuit" based on an argument during prosecution of the '060

patent in which the applicant distinguished its "stacked array dies" from DRAM circuits 206A–D in U.S. Patent Application Publication 2008/0025137 A1 (Ex. 1011 ("Rajan137")). Ex. 2004, 31–32 (citing January 13, 2014 Amendment at 10); *see* Ex. 1002 ('060 prosecution history), 465 (January 13, 2014 Amendment at 10) ("Rajan does not disclose 'a plurality of stacked array dies.' Rajan merely stacks DRAM circuits 206A–D, which are different from array dies.").

Patent Owner argues that we should adopt the district court's construction so that there is a "consistent construction" between the two proceedings. Prelim. Resp. 23–24. Patent Owner, however, qualifies its position by arguing that "the statements it made during prosecution were specific to Rajan137's DRAM circuits 206A–D and this should be made clear to the jury through the order instead of having the expert explain it at trial." Prelim. Resp. 24 n.4 (citing Ex. 2005 (Patent Owner's objections to the district court claim construction order), 1–2); *see* Ex. 2005, 2 ("[T]he Court should make clear that the claimed array die is one that is 'different from Rajan's DRAM circuits 206A–D.'").

Although Patent Owner appears to walk this qualification back by arguing in its Sur-reply that it withdrew its objections to the district court claim construction (Sur-reply 1–2 (citing Exs. 2010, 2011)), Patent Owner's position here still appears to be that the term "array die" is one that is different from DRAM circuits 206A–D of Rajan137. For example, in disputing Petitioner's unpatentability contentions, Patent Owner argues that "the Petition contains no analysis on how or why Kim's or Riho's memory dies are different from Rajan137's DRAM circuits." Prelim. Resp. 26–27; *see also* Prelim. Resp. 27 ("Missing from the Petition is any analysis on why the referenced DRAM dies in Grounds 1 and 2 differ from Rajan137's

(EX1011's) 'DRAM circuits' 206A-D, an analysis that is required under the construction that Petitioner advocated and won in the District Court."). Further, in a district court pleading that Patent Owner cites (Sur-reply 2 (citing Ex. 2008)), Patent Owner argues that "Samsung fails to point to any evidence that its 'DRAM core dies' are or include the 'structural' 'DRAM circuits' of Rajan." Ex. 2008, 3.

Thus, Patent Owner appears to argue that the district court's construction is that the claimed array dies are different from Rajan137's DRAM circuits 206A–D, not all DRAM circuits.

For the reasons explained below in section II.E.3.a, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing under the district court's construction and also under that construction as interpreted by Patent Owner. Because the constructions advocated by Patent Owner do not impact the decision whether to institute, we need not resolve this claim construction issue at this time. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

2. "Chip Select Signals"

Claims 15 and 16 recite "first chip select signals" and "second chip select signals." Patent Owner argues that the district court construed the term "chip select signals" to "exclude[] situations in which a chip select signal could enable multiple array dies at once" and contends that we should adopt this construction. Prelim. Resp. 24–25 (citing Ex. 2004, 33–34). The district court's construction is actually for the "chip select signal" term recited in various claims of the '060 patent. Ex. 2004, 33–34, 36. On this

record, we agree with this interpretation as applied to the "second chip select signals" term of claims 15 and 16 of the '160 patent because these claims recite "the second chip select signals having a number of chip select signals greater than the first chip select signals and *equal to a number of array dies in the plurality of array dies*" (emphasis added). Claims 15 and 16 recite that there are fewer "first chip selection signals" than "second chip selection signals," and, therefore, each of the "first chip selection signals" appears to apply to multiple array dies, which makes sense in the context of the "rank multiplication" of claims 15 and 16.

The parties are free to address these issues further during the trial.

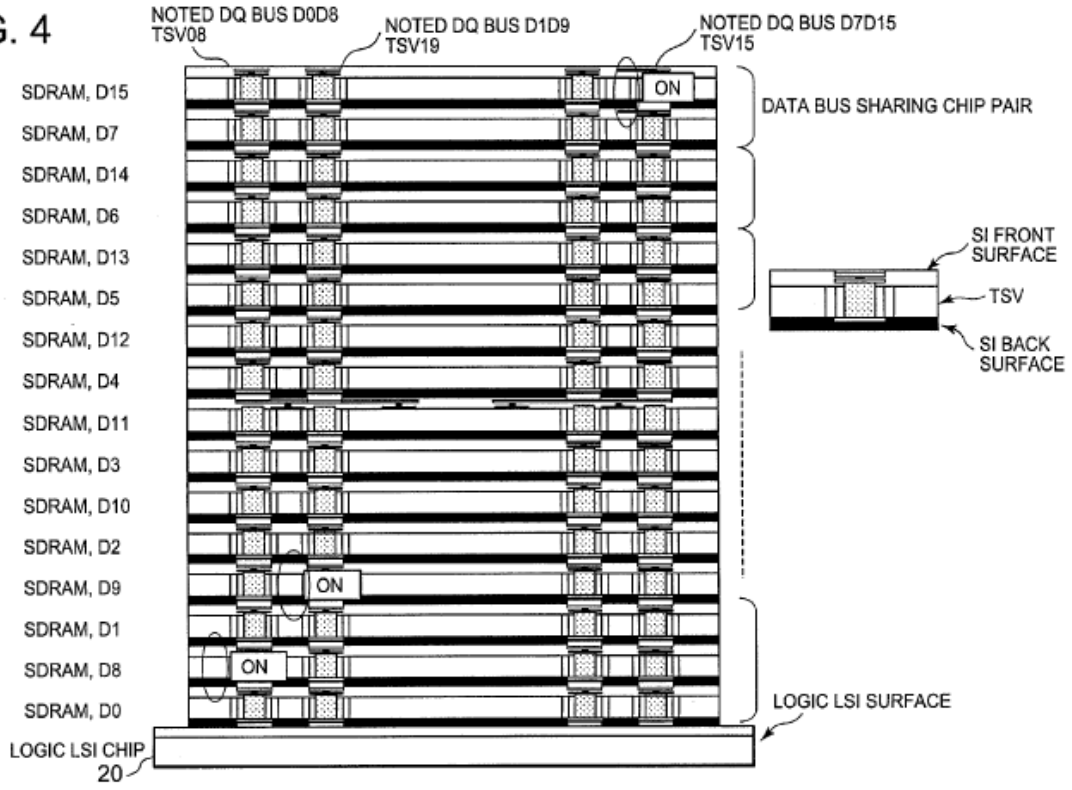
E. Alleged Obviousness over Riho, Rajan, and Riho2 (Claims 1–20)

We begin our analysis with Petitioner's second listed ground in which Petitioner asserts that claims 1–20 are unpatentable as obvious over the combined teachings of Riho, Rajan, and Riho2. Pet. 3, 81–127.

1. Overview of the Prior Art

Riho discloses a memory chip configuration in which memory chips are stacked on a logic chip, such as shown in Figure 4 below.

FIG. 4



Riho's Figure 4 above shows SDRAM chips D0–D15 stacked on LSI logic chip 20 in the following order: D0, D8, D1, D9, D2, D10, D3, D11, D4, D12, D5, D13, D6, D14, D7, D15. Ex. 1016 ¶ 62. SDRAMs D0–D7 form a first group, and SDRAMs D8–D15 form a second group. Ex. 1016 ¶ 62. The adjacent two SDRAMs from each group form a pair, such that D0 and D8 form a pair, D1 and D9 form a pair, and D7 and D15 form a pair. Ex. 1016 ¶ 62. Riho explains that each pair shares a data signal via a through-silicon via (TSV), such that, as illustrated in Figure 4, D0 and D8 share TSV08, D1 and D9 share TSV19, and D7 and D15 share TSV715.[8] Ex. 1016 ¶¶ 62–63. Riho explains that sharing TSVs reduces the load on each SDRAM chip. Ex. 1016 ¶ 103.

[8] Although Figure 4 labels this "TSV15," Riho's written description refers to this as "TSV715." Ex. 1016 ¶¶ 63, 65.

Rajan discloses using an interface circuit to emulate characteristics of particular memory even though the physical memory may not have those characteristics, which allows the "use of low cost memory chips in manufacturing high capacity memory modules." Ex. 1015, 1:51–54, 3:24–43. Rajan explains that the interface circuit may comply with JEDEC standards. Ex. 1015, 4:20–24.

Riho2 discloses adjusting drive capacity of output buffers in memory depending in part on the number of stacked memory chips. Ex. 1018 ¶¶ 10, 96–97.

2. Overview of Petitioner's Contentions for Claim 1

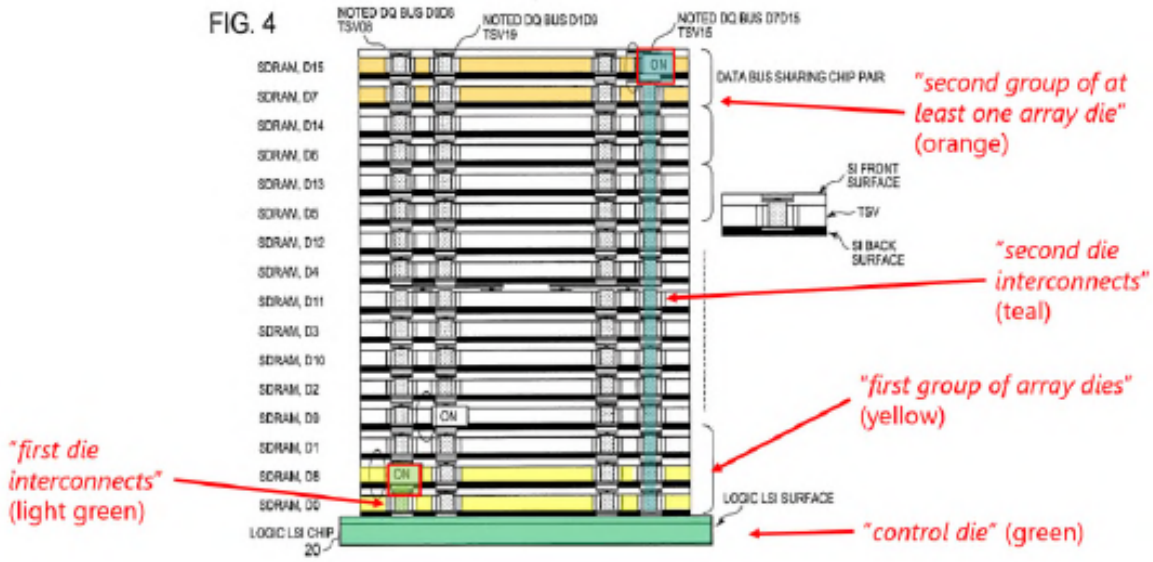
Petitioner argues that Riho discloses a memory package (preamble) having data terminals and control terminals (1.b). Pet. 86–88 (citing Ex. 1016 ¶¶ 26, 30–31, Figs. 1, 2; Ex. 1003 ¶¶ 525–537); *see* Ex. 1016 ¶ 26 (describing, with reference to Figure 1, "external terminals (not illustrated) . . . disposed on the lower side of the logic LSI chip 20"). Petitioner argues that it would have been obvious "to implement Riho's memory package with Rajan's data and control terminals . . . to comply with the JEDEC standards" based on "Rajan's suggestion to implement address, control and data terminals according to JEDEC standards" and because "JEDEC standards were influential and well-known." Pet. 83, 88–90 (citing Ex. 1003 ¶¶ 503–512, 534–535; Ex. 1015, 2:6–7, 3:52–54, 4:20–24, 5:36–43, 6:30–7:67, 8:8–11, Figs. 4, 18).[9]

For element 1.c ("stacked array dies including a first group of array dies and a second group of at least one array die"), Petitioner identifies

[9] Throughout this Decision, we omit the underline emphasis Petitioner provided for the names of the prior art references.

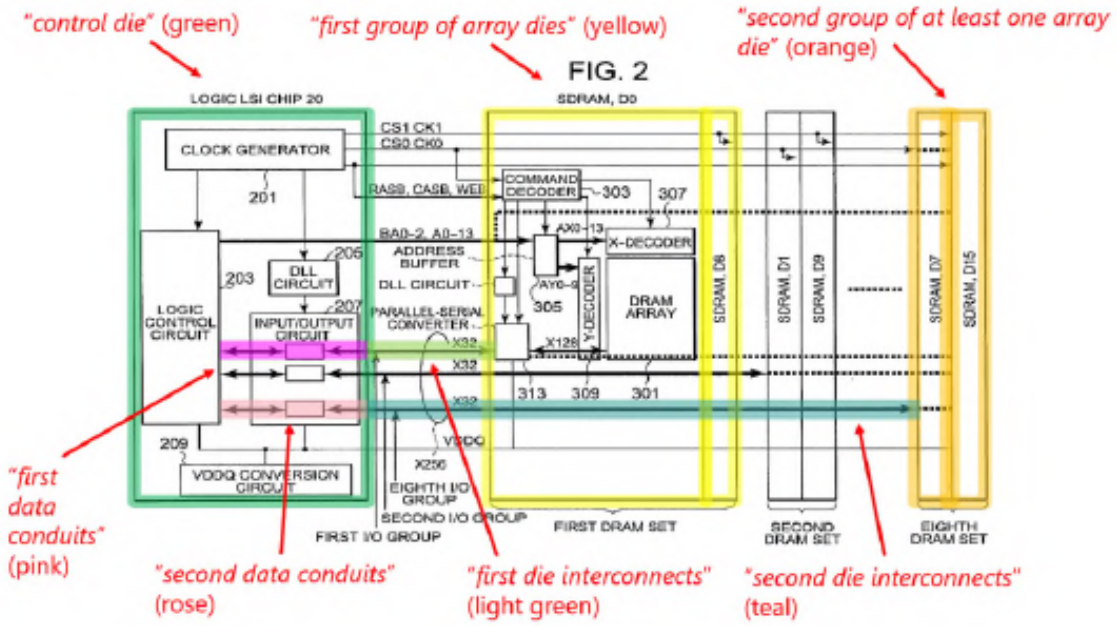
Riho's SDRAM chips D0–D15 as examples of stacked chips each having a die and identifies SDRAMs D0 and D8 as a first group of array dies and SDRAMs D7 and D15 as a second group of array dies. Pet. 90–91 (citing Ex. 1016 ¶¶ 27, 29, 45–47, 49, 62, Figs. 1, 2; Ex. 1003 ¶¶ 538–545; Ex. 1018, code (57), Fig. 1).

For elements 1.d.1 and 1.d.2, Petitioner provides the annotated version of Figure 4 below.



Pet. 92–93. In the annotated version of Figure 4 above, Petitioner identifies TSV08 as the "first die interconnects" in light green and TSV715 as the "second die interconnects" in teal. Pet. 92–93. Petitioner argues that TSV08 is in electrical communication with D0 and D8 ("first group") but not with D7 and D15 ("second group") and that TSV715 is in electrical communication with D7 and D15 but not with D0 and D8. Pet. 92 (citing Ex. 1016 ¶¶ 45–46, 64–65, Figs. 2, 4; Ex. 1003 ¶¶ 546–563). Petitioner argues that "Rajan also teaches this arrangement to reduce load." Pet. 92 (citing Ex. 1015, 5:36–43, 5:63–6:2, Fig. 4; Ex. 1003 ¶¶ 558–562).

For element 1.e.1 ("control die"), Petitioner identifies Riho's logic LSI chip 20. Pet. 94–95 (citing Ex. 1016 ¶ 26, Fig. 1; Ex. 1003 ¶¶ 564–571). Petitioner provides the annotated version of Riho's Figure 2 below to illustrate the first and second data conduits of elements 1.e.2 and 1.e.3.



Pet. 96. Riho's Figure 2 shows logic LSI chip 20 and SDRAM D0 in detail with constituent components and shows other SDRAMs simply as rectangles. Referring to the annotated version of Riho's Figure 2 above, Petitioner argues that the lines colored pink are "first data conduits" that connect data terminals to the "first die interconnects" (light green) and that the lines colored rose are "second data conduits" that connect the data terminals to the "second die interconnects" (teal). Pet. 95–96 (citing Ex. 1016 ¶¶ 26, 39–40, 45–46, Fig. 2; Ex. 1003 ¶¶ 572–588); *see also* Pet. 96–97 (discussing external data terminals for JEDEC-compliant devices).

For elements 1.e.4 and 1.e.5, Petitioner argues that it would have been obvious that the data conduits have drivers to drive the signals that are sent

from input/output circuit 207 in logic LSI chip 20 to SDRAMS D0–D15. Pet. 98–99 (citing Ex. 1016 ¶¶ 40, 45–46; Ex. 1030, 135–36; Ex. 1038, 68; Ex. 1003 ¶¶ 589–606). Petitioner argues that Riho teaches that varying impedances between TSVs that result from, for example, manufacturing processes and chip placement, should be taken into account. Pet. 99–100 (citing Ex. 1016 ¶¶ 55–56, 61); *see* Ex. 1016 ¶ 61 (discussing that the chip located closest to the control chip has "smaller penetrating through resistance" than a chip farther from the control chip). Petitioner contends that a person of ordinary skill "would have been motivated by Riho2 to account for these variations by selectively activating one or more drivers . . . to achieve the optimal driving strength for each 'data conduit,' thus saving power." Pet. 100 (citing Ex. 1018 ¶¶ 96–97, Fig. 7A; Ex. 1017, 1:22–24, 5:11–14, Fig. 5; Ex. 1003 ¶¶ 598–603); *see also* Pet. 100–01 (asserting that "[o]ther contemporaneous references confirm that adjusting the driver strength to account for the position of a die in stack was well known at the time" (citing Ex. 1039, code (57), 7:46–49, Fig. 6)).

3. Patent Owner's Arguments and Our Preliminary Analysis

Patent Owner makes two arguments against Petitioner's challenge to claim 1 based on the combination of Riho, Rajan, and Riho2, which we address below.

a) Element 1.c ("array dies")

Patent Owner disputes Petitioner's showing for element 1.c's "array dies." Prelim. Resp. 26–31. According to Patent Owner, "the Petition contains no analysis on how or why . . . Riho's memory dies are different from Rajan137's DRAM circuits, an interpretation that it advocated and persuaded the District Court to adopt." Prelim. Resp. 26–27. On this record, however, we see nothing to indicate that Riho's SDRAM chips

D0–D15 are the same as Rajan137's DRAM circuits. We note at least one difference is that Riho discloses that each of D0–D15 is a 2 Gbit memory (Ex. 1016 ¶¶ 35, 47) whereas Rajan137 states that "the stack of DRAM circuits 206A-D may include eight 512 Mb DRAM circuits . . . to resemble a single 4 Gb DRAM circuit" (Ex. 1011 ¶ 45).

Furthermore, to the extent the claim excludes any DRAM chips at all, Riho explains that its disclosures are not limited to SDRAM. Ex. 1016 ¶ 135; *see* Reply 4. Patent Owner counters that Petitioner "relies on ***DRAM*** JEDEC standards and textbooks . . . and compliance thereof by *e.g.*, . . . Riho, to argue that the limitations are met." Sur-reply 3. Petitioner's contention, however, is that it would have been obvious "to create a package with an *interface* that complied with the well-known JEDEC standards." Pet. 83 (emphasis added); *see also* Pet. 84 ("Such a combination would have been well within a [person of ordinary skill in the art]'s level of skill since *emulating* a standard JEDEC interface was well-known, as demonstrated by Rajan . . . and the 160 Patent's admitted prior art . . . ." (emphasis added)). Thus, on this record, we do not agree with Patent Owner that Petitioner's reliance on JEDEC compliance undermines Petitioner's contentions.

For the reasons given by Petitioner and those discussed above, we are sufficiently persuaded that Riho teaches the subject matter of element 1.c applying the district court's construction of "array die" and applying Patent Owner's interpretation of the district court's construction.

b) Elements 1.d.1 and 1.d.2 ("not in electrical communication")

Second, Patent Owner argues that Petitioner's contentions fail for elements 1.d.1 and 1.d.2 because each of the TSVs ("die interconnects") is electrically connected to a switch circuit on each die such that Riho does not

teach die interconnects that are "not in electrical communication" with certain array dies as recited in claim 1. Prelim. Resp. 37–38 (citing Ex. 1016 ¶ 45, Figs. 4–6). Patent Owner argues that there is no data exchange with certain chips because the switches on those chips are turned off, not because the TSVs have no electrical connection to the chips. Prelim. Resp. 38–39 (citing Ex. 1016 ¶¶ 72–75, 91, Fig. 5). Patent Owner further argues that "Petitioner does not explain . . . how Riho's structure differs from a conventional multi-drop architecture" as allegedly disclosed in the prior art configuration of Figure 1A of the '160 patent. Prelim. Resp. 40.

On the present record, we find Petitioner's contentions sufficiently persuasive. Riho describes the TSV configuration as follows: "[T]he data signal DQ TSV19 and circuits formed at the front surfaces of the SDRAMs D1 and D9 are in a conductive state (i.e. on state) while the data signal DQ TSV19 is *not electrically connected to the SDRAMs other than the SDRAMs D1 and D9*." Ex. 1016 ¶ 65 (emphasis added); *see* Pet. 92 (citing this disclosure). Thus, Riho expressly discloses that there is no electrical connection to SDRAMs other than the pair with which the TSV is in a "conductive state." On this record, we disagree with Patent Owner's argument that Riho's use of a switch to accomplish this is no different from the prior art configuration in Figure 1A of the '160 patent. *See* Prelim. Resp. 40. In describing the state of the prior art, the '160 patent explains that "a load exists on each of the drivers 134, 140, 184, and 186 by virtue of the drivers being in electrical communication with the corresponding die interconnects *and the corresponding circuitry of the array dies*," which requires a driver "large enough to overcome the load on the driver." Ex. 1001, 2:10–15 (emphasis added). Riho does not present the same issue because the TSVs are "not electrically connected to" all of the SDRAMs, as

explained in paragraph 65 of Riho, thus obviating the need for drivers large enough to drive signals to all of the circuitry on all chips.

Patent Owner states that Petitioner "argued in the District Court that a TSV is in electrical communication with an SDRAM die even if the driver/receiver circuit for the associated memory arrays on the die is turned off." Prelim. Resp. 39. Patent Owner, however, does not cite any support for this assertion. In its Sur-reply, Patent Owner cites an email allegedly showing that Petitioner regards Riho as a non-infringing alternative. Sur-reply 4 (citing Ex. 2012). On this record, however, we do not view this position as inconsistent with Petitioner's contentions in this proceeding, which are based on obviousness, not anticipation. *Cf. Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1378 (Fed. Cir. 2001) ("[I]t is axiomatic that that which would literally infringe if later anticipates if earlier.").

For the reasons given by Petitioner and those discussed above, we are sufficiently persuaded that Riho teaches die interconnects that are "not in electrical communication" with certain array dies and that the asserted combination renders obvious the subject matter of elements 1.d.1 and 1.d.2.

4. Preliminary Determination for Claim 1

For the reasons discussed above and based on Petitioner's contentions and evidence, summarized above, we are persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claim 1 is unpatentable as obvious over the combined teachings of Riho, Rajan, and Riho2.

5. Claims 2–14 and 17–20

Petitioner asserts that independent claims 6 and 10 and dependent claims 2–5, 7–9, 11–14, and 17–20 are unpatentable as obvious over the

combined teachings of Riho, Rajan, and Riho2. Pet. 101–19, 125–27. Patent Owner relies on the arguments addressed above in § II.E.3 for claims 2–14 and 17–20 and does not set forth additional arguments for these claims at this stage of the proceeding. We have reviewed Petitioner's contentions, and we are sufficiently persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claims 2–14 and 17–20 are unpatentable as obvious over the combined teachings of Riho, Rajan, and Riho2.

6. Claims 15 and 16

Petitioner asserts that dependent claims 15 and 16 are unpatentable as obvious over the combined teachings of Riho, Rajan, and Riho2. Pet. 119–25. For these claims, we focus on the disputed issue between the parties, which is whether the asserted prior art teaches "chip select signals" as recited in these claims. Prelim. Resp. 48–50.

Petitioner argues that it would have been obvious to have the number of chip select signals equal the number of array dies based on Rajan's disclosure of "utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack" (Ex. 1015, 6:34–38). Pet. 120 (citing Ex. 1003 ¶¶ 784–791); *see also* Pet. 121 (asserting that "the JEDEC standard required separate chip-select signals for each stacked memory chip").

Patent Owner argues that Riho has only two chip select signals, CS0CK0 and CS1CK1, each of which selects multiple dies. Prelim. Resp. 48–49 (citing Ex. 1016 ¶ 37, Fig. 2). This argument, however, does not address Petitioner's contentions based on Rajan's disclosure of using separate chip select signals for each DRAM chip. Ex. 1015, 6:34–38.

For the reasons given by Petitioner and those discussed above, we are sufficiently persuaded that the subject matter of claims 15 and 16 reciting "a

number of chip select signals . . . equal to a number of array dies in the plurality of array dies" would have been obvious to a person of ordinary skill in the art based on the combination of Riho, Rajan, and Riho2.

We are sufficiently persuaded, on this record, that Petitioner shows a reasonable likelihood of prevailing in demonstrating that claims 15 and 16 are unpatentable as obvious over the combined teachings of Riho, Rajan, and Riho2.

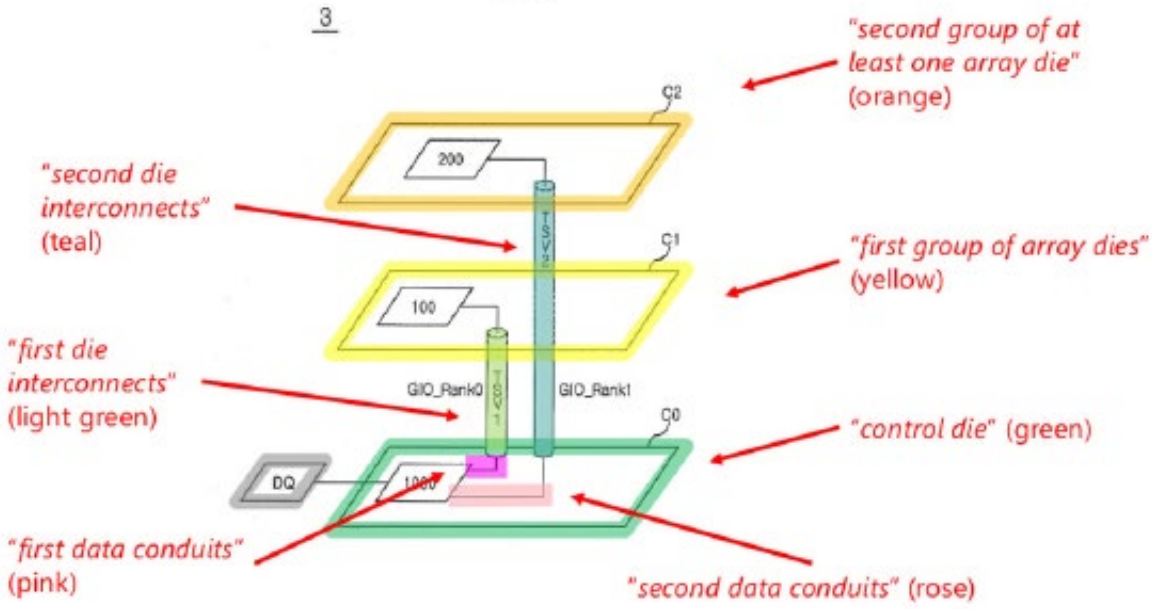
F. Alleged Obviousness over Kim, Rajan, and Wyman (Claims 1–20)

Petitioner asserts that claims 1–20 are unpatentable as obvious over the combined teachings of Kim, Rajan, and Wyman. Pet. 3, 23–80. Having determined that the Petition meets the threshold for institution (reasonable likelihood of prevailing as to at least one of the challenged claims) based on the combination of Riho, Rajan, and Riho2, the remainder of this Decision focuses on the parties' disputes to provide guidance to the parties for the trial.

1. Overview of Petitioner's Contentions for Claim 1

To illustrate its contentions based on Kim, Petitioner provides the following annotated version of Kim's Figure 5:

FIG.5



Pet. 34. Kim's Figure 5 depicts main chip C0 with TSVs connecting C0 to each of stacked memory chips C1 and C2. Ex. 1014 ¶ 48. In the annotated figure above, Petitioner maps depicted components to elements of claim 1 as follows: chip C1 (yellow) as "first group of array dies"; chip C2 (orange) as "second ground of at least one array die"; chip C0 (green) as "control die"; TSV1 (light green) from C0 to C1 as "first die interconnects"; TSV2 (teal) from C0 to C2 as "second die interconnects"; box labeled "DQ" (gray) as "data terminals"; line (pink) from data input/output section 1000 to TSV1 as "first data conduits"; and line (rose) from data input/output section 1000 to TSV2 as "second data conduits." Pet. 34–53.

Petitioner argues that a person of ordinary skill in the art would have been motivated to make Kim's memory package compatible with JEDEC standards based on Rajan's teachings. Pet. 26–29. Petitioner also argues that a person of ordinary skill in the art would have been motivated to have multiple memory chips share a TSV because this was a known option and "would not require creating new TSVs (which would add space and

circuitry) and would allow emulating the JEDEC standard required by external devices." Pet. 30–31. Petitioner relies on Wyman to teach using different driver sizes depending on load. Pet. 32–33.

2. Patent Owner's Arguments for Claim 1

a) Element 1.c ("array dies")

As to element 1.c regarding the recited "array dies," Patent Owner argues that Petitioner has not shown that Kim's or Rajan's memory dies are different from Rajan137's DRAM circuits, which Patent Owner asserts are excluded from the scope of the claim. Prelim. Resp. 21–23, 26–31. On this record, we disagree. As Petitioner correctly points out, Kim does not even mention DRAM and thus is not limited to DRAM. *See* Reply 3. Furthermore, as Petitioner points out (Reply 2–3), Rajan states that "any type of memory whatsoever" may be used in its disclosure and lists non-DRAM memories. Ex. 1015, 15:3–9. Patent Owner argues that Rajan137 also states that its disclosure applies to memory types other than DRAM, which, according to Patent Owner, shows that Rajan and Rajan137 are the same in this respect. Sur-reply 2–3 (citing Ex. 1011 ¶¶ 18, 43). But the arguments during prosecution of the '060 patent specifically cited Rajan137's "DRAM circuits 206A–D," not other types of memory. Ex. 1002, 465. Therefore, to the extent there was disclaimer of subject matter during prosecution (*see* Prelim. Resp. 12–15, 21–24), it would appear to be disclaimer of Rajan137's "DRAM circuits 206A–D," not a disclaimer of all memory chips.

Patent Owner also argues that Petitioner "relies on ***DRAM*** JEDEC standards and textbooks . . . and compliance thereof by *e.g.*, Kim[or] Rajan . . . , to argue that the limitations are met." Sur-reply 3. But as discussed above in section II.E.3.a for a similar argument as to Riho,

Petitioner's contention is that it would have been obvious "to create a package with an *interface* that complied with the well-known JEDEC standards." Pet. 26 (emphasis added); *see also* Pet. 27–28 (asserting that "emulating a standard JEDEC interface was a known option"). Thus, on this record, we do not agree with Patent Owner that Petitioner's reliance on JEDEC compliance undermines Petitioner's contentions.

On this record, we are sufficiently persuaded by Petitioner's contentions that the combination of Kim, Rajan, and Wyman teaches "array dies" that are "different from a DRAM circuit," as in the district court's construction, and also that are different from Rajan137's DRAM circuits 206A–D, as in Patent Owner's interpretation of the district court's construction.

b) Operability of modified Kim

Patent Owner also argues that Petitioner has not shown how including additional dies connected to the same TSV in Kim would result in an operable device and that there is "no competent evidence" to support the operability of the combination. Prelim. Resp. 31–37 (emphasis omitted). On this record, we disagree. As Petitioner points out (Pet. 40), Kim discloses that "any number of" memory chips may be used and that "a person having ordinary skill in the art will appreciate that the technical concept of the present invention can be applied to a semiconductor memory apparatus . . . divided into three or more ranks." Ex. 1014 ¶¶ 48, 50. In support of its contentions, Petitioner points to Rajan's disclosure of multiple stacked memory chips connected to the same data bus. Pet. 41–42 (citing Ex. 1015, Fig. 4; Ex. 1003 ¶¶ 206–212). Petitioner also cites another reference that Petitioner asserts "show[s] multiple groups of stacked dies, where each die in a group is connected to the same data interconnect."

Pet. 40–41 (citing US 7,796,446 B2, filed Sept. 19, 2008 (Ex. 1024, "Ruckerbauer"), 9:14–18, Fig. 5). Ruckerbauer discloses a memory stack in which two memory dies are connected to data transfer path 12a and three memory dies are connected to data transfer path 12b. Ex. 1024, 9:4–18, Fig. 5. Patent Owner cites Ruckerbauer's disclosure of "internal signal paths" and argues that "dies belonging to the same rank each have a different signaling pathway." Prelim. Resp. 35 (citing Ex. 1024, 10:60–62, 10:64–67). On this record, we do not see that this disclosure undermines Ruckerbauer's express disclosure of multiple memory dies sharing one transfer data path, discussed above.

Based on the foregoing, we are sufficiently persuaded by Petitioner's evidence that it would have been within the knowledge and skill of a person of ordinary skill in the art to connect multiple memory chips to Kim's TSVs in a manner that is operable. *See* Ex. 1003 ¶¶ 204–212.

3. Claims 15 and 16

Similar to its arguments for the Riho ground discussed above in section II.E.6, Petitioner argues that Rajan teaches using separate chip select signals for each memory chip in a stack and that JEDEC requires this. Pet. 73 (citing Ex. 1015, 6:34–38), 74–75. Patent Owner argues that Petitioner's contentions for claims 15 and 16 fail because the chip select signal in the proposed combination would select more than one chip, contrary to the district court's construction. Prelim. Resp. 43–48. More particularly, Patent Owner argues that, "according to Petitioner's own evidence, a JEDEC-compliant chip select signal that it claims a [person of ordinary skill in the art] would have installed in modified Kim would select an entire rank of DRAM devices," i.e., multiple DRAM devices. Prelim. Resp. 47. Petitioner argues that its position is that "***each*** die in the group is

in a ***separate*** rank and receives a ***separate*** 'chip select signal,'" consistent with the Petition's discussion of both JEDEC and Rajan disclosing separate chip select signals for each chip in a stack. Reply 5–6 (citing Pet. 74–76). Patent Owner counters that "the Reply does not explain where in the Petition it argues that each die in the modified Kim (where a TSV is connected to more than one die) belongs to a separate rank or receives a separate chip select signal." Sur-reply 5.

As discussed in section II.D.2 above, claims 15 and 16 recite "the second chip select signals having a number of chip select signals . . . equal to a number of array dies in the plurality of array dies." To the extent Patent Owner is correct that a JEDEC-compliant chip select signal selects multiple chips and thus does not meet the language of the claims, Petitioner's reliance on the JEDEC standard may, on its own, be insufficient to show obviousness. Petitioner, however, also relies on Rajan's disclosure of "utilizing separate chip select signals (not shown) to each of the DRAM chips in the stack" (Ex. 1015, 6:34–38). Pet. 73 (citing Ex. 1003 ¶¶ 443–450). Thus, we disagree with Patent Owner's contention that Petitioner has not shown "where in the Petition it argues that each die in the modified Kim (where a TSV is connected to more than one die) belongs to a separate rank or *receives a separate chip select signal*." *See* Sur-reply 5 (emphasis added).

4. Preliminary Determination for Claims 1–20

We have reviewed Petitioner's contentions based on the combination of Kim, Rajan, and Wyman and find them sufficiently persuasive on this record.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented in the Petition establishes that there is a reasonable likelihood that Petitioner would prevail in challenging at least one claim of the '160 patent, and we institute *inter partes* review of all challenged claims on all grounds raised in the Petition. *See* 37 C.F.R. 42.108(a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim."). At this stage of the proceeding, we have not made a final determination with respect to the patentability of any of the challenged claims or the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a) and 37 C.F.R. § 42.4, an *inter partes* review is hereby instituted as to claims 1–20 of the '160 patent on all challenges raised in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which will commence on the entry date of this decision.

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Paper 10
Date: December 7, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00996
Patent 11,016,918 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and NABEEL U. KHAN, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1–30 of U.S. Patent 11,016,918 B2, issued on May 25, 2021 (Ex. 1001, "the '918 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.") to the Petition.

Institution of an *inter partes* review is authorized when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

Based on the current record, and for the reasons explained below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one challenged claim, and we institute an *inter partes* review as to all the challenged claims and grounds raised in the Petition.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 1. Patent Owner identifies itself as the sole real party in interest. Paper 4, 1.

B. Related Matters

The parties advise that the '918 patent is related to *Samsung Electronics Co., Ltd., et al. v. Netlist, Inc.*, IPR2022-00999 (U.S. Patent No. 11,232,054 B2; *Netlist, Inc. v. Samsung Electronics Co., Ltd., et al.*, Case No. 2-21-cv-00463 (E.D. Tex.); *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, Case No. 1:21-cv-01453 (D. Del.); and U.S. Appl. No. 17/582,797. Pet. 1; Paper 4, 1.

The parties advise that the '918 patent is related to the following legal proceeding, which is no longer pending: *SK hynix Inc. v. Netlist, Inc.*, IPR2017-00692 (U.S. Patent No. 8,874,831 B2). Pet. 1; Paper 4, 1.

C. The '918 Patent (Ex. 1001)

The '918 patent is titled "Flash-DRAM Hybrid Memory Module." Ex. 1001, code (54). Figure 12 of the '918 patent is reproduced below.

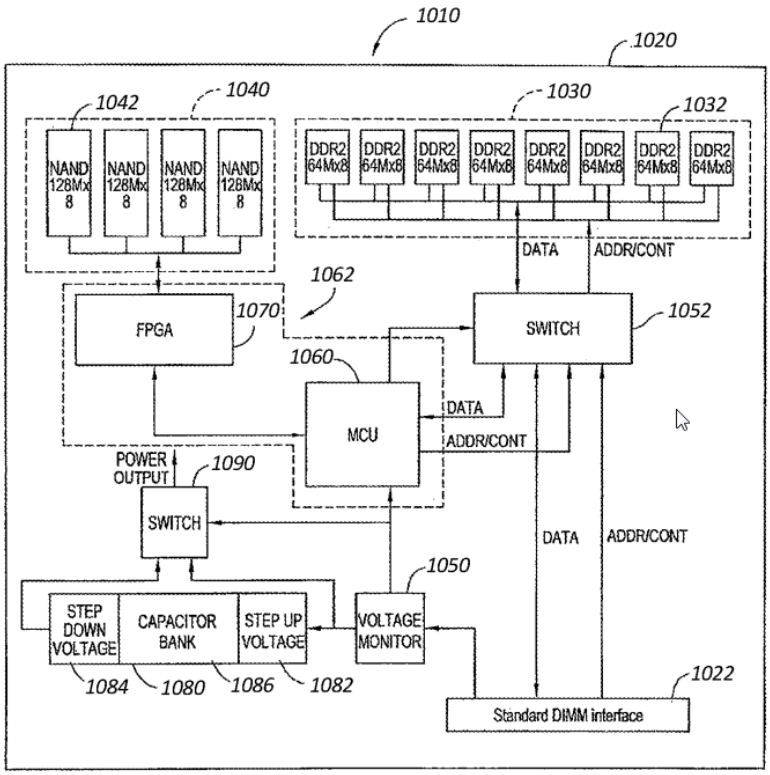


FIG. 12

Figure 12 shows an example memory system 1010 of the '918 patent. *Id.* at 21:14–16. The memory system 1010 includes a volatile memory subsystem 1030, a non-volatile memory subsystem 1040, and a controller 1062 operatively coupled to the volatile memory subsystem 1030 and selectively coupled to the non-volatile memory subsystem 1040. *Id.* at 21:16–22. Volatile memory 1030 may comprise elements 1032 of two or more dynamic random access memory (DRAM) elements such as double data rate (DDR), DDR2, DDR3, and synchronous DRAM (SDRAM). *Id.* at 22:16–19. Non-volatile memory 1040 may comprise elements 1042 of flash memory elements such as NOR, NAND, ONE-NAND flash and multi-level

cell (MLC). *Id.* at 22:35–40. Memory system 1010 may comprise a memory module or printed circuit board (PCB) 1020. *Id.* at 21:24–26. Memory system 1010 has an interface 1022 for power voltage, data, address, and control signal transfer between memory system 1010 and a host system. *Id.* at 22:3–6.

Controller 1062 may include microcontroller unit 1060 and FPGA logic 1070, either as separate devices or integrated together. *Id.* at 24:35–37, 23:19–22, Fig. 14. Microcontroller 1060 may transfer data between the volatile memory 1030 and non-volatile memory 1040. *Id.* at 24:35–41. Logic element 1070 provides signal level translation and address translation between the volatile memory and the non-volatile memory. *Id.* at 24:45–56.

When the system is operating normally, controller 1062 controls switch 1052 to decouple the volatile memory 1030 from controller 1062 and the non-volatile memory 1040 (the '918 patent refers to this as the "first state."). *Id.* at 24:60–25:7. In response to a power interruption, for example, controller 1062 controls switch 1052 to couple the volatile memory 1030 to itself and non-volatile memory 1040, and transfers data from the volatile memory to the non-volatile memory to prevent its loss (the '918 patent refers to this as the "second state"). *Id.* at 25:9–20.

Memory system 1010 may comprise a voltage monitor 1050 to monitor voltage supplied from the host system via interface 1022. *Id.* at 25:8–10. When the voltage monitor 1050 detects a low voltage condition, the voltage monitor transmits a signal to the controller 1062 to indicate the detected condition. *Id.* at 25:11–15.

Power may be supplied from a first power supply (e.g. a system power supply) when the memory system 1010 is in the first state and from a second

power supply 1080 when the memory system 1010 is in the second state. *Id.* at 25:54–58. Second power supply 1080 may comprise step-up transformer 1082, step-down transformer 1084, and capacitor bank 1086 with one or more capacitors. *Id.* at 26:3–13.

The memory system 1010 further has a third state in which controller 1062 is decoupled from the volatile memory system 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). *Id.* at 25:62–69. "[T]he third power supply may provide power to the volatile memory subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred." *Id.* at 25:66–26:3.

Figure 16 of the '918 patent is reproduced below.

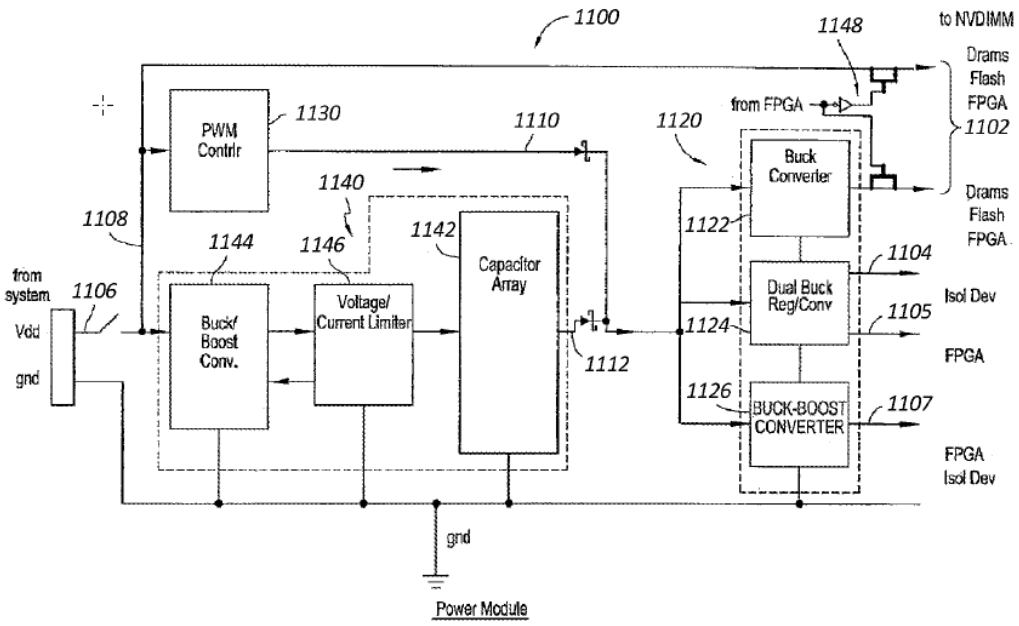


FIG. 16

Figure 16 shows power module 1100 of memory system 1010. *Id.* at 27:59–61. Power module 1100 comprises conversion element 1120, first power element 1130, and second power element 1140. *Id.* at 28:7–15,

28:20–22. Conversion element 1120 comprises sub-blocks 1122, 1124, 1126 comprised of various converter circuits such as buck converters, boost converters, and buck-boost converters for providing various voltages 1102, 1104, 1105, 1107 from the outputs of the first and second power elements 1130, 1140. *Id.* at 29:18–54. The first power element 1130 may comprise a pulse-width modulation power controller generating voltage 1110 from voltages 1106, 1108. *Id.* at 28:13–15. Second power element 1140 may comprise capacitor array 1142, buck-boost converter 1144 receiving voltages 1106, 1108 and adjusting the voltage for charging the capacitor array, and voltage/current limiter 1146, which limits charge current to the capacitor array and stops charging the capacitor array 1142 when it reaches a certain charge voltage. *Id.* at 28:62–67. "[P]ower module 1100 provides power to [ ] components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition." *Id.* at 27:61–65.

Specifically, "[i]n a first state, first voltage 1102 is provided to memory system 1010 from input 1106 and fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130." *Id.* at 28:27–31. "In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120." *Id.* at 28:32–37. "In the third state, the fifth voltage 1112 is provided to conversion element 1120 from second power element 1140 and the first voltage 1104 is provided to memory system 1010 from conversion element 1120." *Id.* at 28:34–38. Transition from the first state to the second state may occur when power module 1100 detects a power failure is about to

occur, and transition from the second state to the third state may occur when it detects a power failure has occurred. *Id.* at 28:39–47.

D. Illustrative Claim

Of the challenged claims, claims 1, 16, and 23 are independent. Independent claim 1, reproduced below with brackets noting Petitioner's identifiers, is illustrative of the claimed subject matter.

> 1. [1.a] A memory module comprising:
> [1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
> [1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
> [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
> [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
> [1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
> [1.g] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
> [1.h] a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
> [1.i] [1.i.1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, [1.i.2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, [1.i.3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, [1.i.4] wherein a first one of the second and fourth voltage

amplitudes is less than a second one of the second and fourth voltage amplitudes.

Ex. 1001, 38:19–44.

E. Evidence

Petitioner relies on the following references (*see* Pet. 3, 10–14), as well as the Declaration of Dr. Andrew Wolfe (Ex. 1003).

Reference	Exhibit No.	Patent/Printed Publication
Harris	1023	U.S. Patent Pub. No. 2006/0174140 A1 to Harris, published August 3, 2006
Amidi	1024	U.S. Patent No. 7,724,604 B2, issued May 25, 2010
Spiers	1025	U.S. Patent Pub. No. 2006/0080515 A1, published Apr. 13, 2006
FBDIMM Standards	1027, 1028	JESD82-20 and JESD205 standards published March 2007
Hajeck	1038	U.S. Patent No. 6,856,556 B1 to Hajeck, issued Feb. 15, 2005

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–30 are unpatentable on the following Grounds (Pet. 4):

Claims Challenged	35 U.S.C. §	References
1–3, 8, 14, 15, 23	103(a)	Harris, FBDIMM Standards
1–30	103(a)	Harris, FBDIMM Standards, Amidi
1–30	103(a)	Harris, FBDIMM Standards, Amidi, Hajeck
1–30	103(a)	Spiers, Amidi
1–30	103(a)	Spiers, Amidi, Hajeck

III. ANALYSIS OF CHALLENGED GROUNDS

We turn now to Petitioner's asserted grounds of unpatentability and Patent Owner's arguments in its Preliminary Response to determine whether Petitioner has met the threshold standard of 35 U.S.C. § 314(a).

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations.[1] *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see also KSR*, 550 U.S. at 418. Further, an assertion of obviousness "cannot be sustained by mere

[1] Neither party has identified any objective evidence of nonobviousness on the record to be considered at this time.

conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'").

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3)); *see also Intelligent Bio-Sys.*, 821 F.3d at 1369 ("It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'" (quoting 35 U.S.C. § 312(a)(3))). Therefore, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable. At this preliminary stage, we determine whether the information presented in the Petition shows there is a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims would have been obvious over the proposed combinations of prior art.

A. Level of Ordinary Skill in the Art

Petitioner asserts a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field." Pet. 8–9 (citing Ex. 1003 ¶ 67). Petitioner contends that additional training can substitute for educational or

research experience, and vice versa. *Id.* at 8. Petitioner asserts that such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. *Id.* at 8–9. Petitioner further contends that such "a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers." *Id.* at 9. Petitioner further asserts that such "a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry." *Id.*

In the Preliminary Response, Patent Owner applies the level of ordinary skill in the art proposed by Petitioner. Prelim. Resp. 6.

Among the factors that may be considered in determining the level of ordinary skill in the art are "the type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962–63 (Fed. Cir. 1986)). The evidence presented mostly applies to the educational level of workers in the field, but also touches upon other factors

as well. We find Petitioner's proposal is consistent with the level of ordinary skill in the art reflected by the '918 patent and the prior art of record, and we, therefore, adopt Petitioner's proposed level of ordinary skill in the art, with the exception of the open-ended language "at least," for purposes of this Decision.

B. Claim Construction

We construe each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent," the same standard used to construe the claim in a civil action. 37 C.F.R. § 42.100(b).

Petitioner contends that "no express constructions are needed for this proceeding" but notes that Patent Owner has broadly interpreted some claim terms for purposes of infringement even though a narrower interpretation may be more reasonable. Pet. 9 (citing Ex. 1071, 39–46; Ex. 1073, 46–63; Ex. 1003 ¶ 128). Petitioner further contends it is not necessary to determine whether claim terms are governed by § 112, 6th paragraph because at least one of the prior art combinations matches the disclosure of the '918 patent. *Id.*

At this stage in the proceeding, we need only construe the claims to the extent necessary to determine whether to institute *inter partes* review. *See Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1375 (Fed. Cir. 2019) ("The Board is required to construe 'only those terms . . . that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). We determine that, at this stage of this proceeding, there is no need to expressly construe any claim terms in order to determine

whether or not to institute review because the parties do not dispute the claimed terms' meanings, and their ordinary and customary meanings suffice for our analysis. However, we do invite the parties to construe the term "pre-regulated voltage" at trial for reasons explained in Section III.D.4, *infra*.

C. Ground 1: Obviousness Over Harris and FBDIMM Standards

Petitioner contends claims 1–3, 8, 14, 15, and 23 would have been obvious over the combination of Harris and FBDIMM Standards and relies on the Declaration of Dr. Andrew Wolfe (Ex. 1003) in support. Pet. 14–51. For the reasons that follow, we are persuaded that the evidence, including Dr. Wolfe's testimony, sufficiently supports Petitioner's arguments and, therefore, establishes a reasonable likelihood of prevailing with respect to this ground at this stage of the proceeding.

1. Harris (Ex. 1023)

Harris is titled "Voltage Distribution System and Method for a Memory Assembly." Ex. 1023, code (54). Harris was published as U.S. Patent Pub. No. 2006/0174140 A1 on August 3, 2006. Petitioner contends Harris is prior art under § 102(a). Pet. 10.

Harris's Figure 1A is reproduced below.

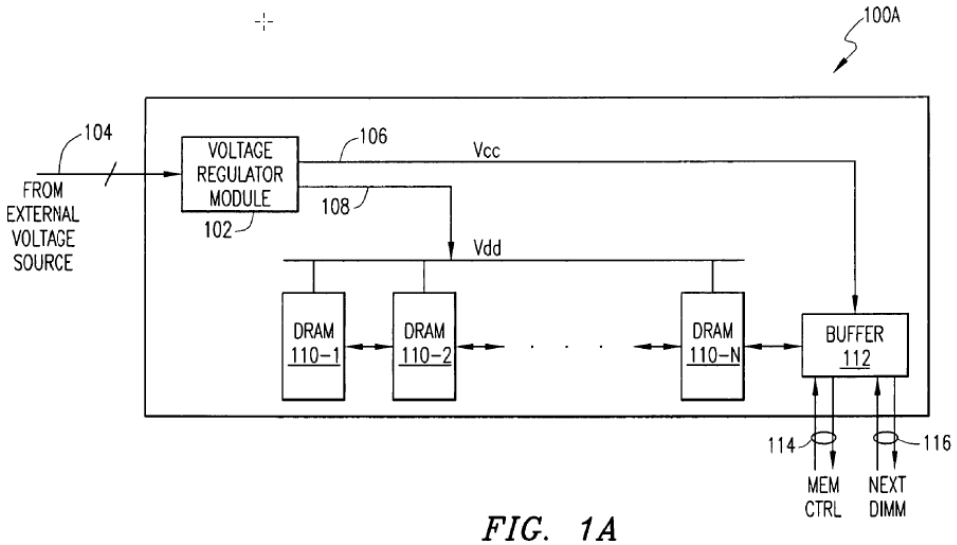


FIG. 1A

As shown in Figure 1A, Harris discloses a memory module 100A including on-board regulator 102 for converting an externally supplied voltage 104 to appropriate local voltage levels 106 (V_{cc}), 108 (V_{dd}), such as 0.5V to 3.5V. Ex. 1023, code (57), ¶¶ 9–10. Voltage 106 is supplied to buffer/logic component 112 which may be connected to a memory controller via interface 114 and daisy-chained with other memory assemblies via interface 116. *Id.* ¶ 9. Voltage 108 powers memory devices 110-1 to 110-N. *Id.* The memory module 100A may be a Dual In-Line Memory Modules (DIMM) wherein each of the memory devices 100-1 to 100-N comprises a Double Data Rate (DDR), DDR2, or DDR3 device. *Id.* The memory module 100A may be an unbuffered, registered or fully buffered DIMM. *Id.*

2. FBDIMM Standards (Exs. 1027, 1028)

In March 2007, the Joint Electron Device Engineering Council (JEDEC) published standards for Fully Buffered DIMM (FBDIMM) memory modules titled "JESD82-20" (Ex. 1027) and "JESD205" (Ex. 1028). Ex. 1029 ¶¶ 134–137. Petitioner refers to these standards

collectively as the "FBDIMM Standards." Pet. 11. Petitioner contends the FBDIMM Standards are prior art under § 102(a). *Id.*

The FBDIMM Standards specify voltages for components on the memory module as follows:

Product Family Attributes

DIMM organization	x72 ECC			
DIMM dimensions (nominal)	30.35mm (height) x 133.35mm (width) x 8.2 mm (max thickness) MO-256 variation AB 30.35mm (height) x 133.35mm (width) x 8.8 mm (max thickness) MO-256 variation BB			
Pin count	240			
SDRAMs supported	256Mb, 512Mb, 1Gb, 2Gb, 4Gb			
Capacity	256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB			
Serial PD	Consistent with JC 45			
Supply voltages (nominal)	min	typ	max	
	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})
Buffer Interface	High-speed Differential Point-to-point Link at 1.5 volt			
DRAM Interface	SSTL_18			

Note 1: Approximate DC values, refer to AMB Component Specification for actual DC and AC values and conditions.
Note 2: Vtt range accomodates measurable offset due to complementary CA bus current paths. (See Vtt section)
An Unloaded system should supply Vtt of 0.48*Vdd/0.52*Vdd to Dimm socket

Ex. 1028, 9. The above table shows values for supply voltages including DRAM V_{DD}, AMB V_{CC}, DRAM interface V_{TT}, and V_{DDSPD}. The FBDIMMM Standards further specify the following voltages for various power supplies:

Table 9.2 — Pin Description (Sheet 3 of 3)

Signal	Type	Description
$\overline{\text{RESET}}$		Power Good Reset
Miscellaneous Test		
TEST (4 pins)	NC	Pin for debug and test. Must be floated on DIMM.
TESTLO (5 pins)	A	Pin for debug and test. Must be tied to Ground on DIMM
TESTLO_AB20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
TESTLO_AC20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes
Other Pins		
BFUNC	I	**Buffer Function Bit:** When BFUNC = 0, AMB is used as a regular buffer on FB-DIMM. When BFUNC = 1, AMB is used as either a repeater or a buffer for LAI function. On FB-DIMM, BFUNC is tied to Ground
RFU (18 pins)	NC	**Reserved for Future Use.** Must be floated on DIMM. RFU pins denoted by "a" are reserved for forwarded clocks in future AMB implementations.
Other No Connect Pins		
NC (129 pins)	NC	No Connect pins

Ex. 1027, 83. The table above sets voltage levels for power supplies V_{CC}, V_{CCFBD}, V_{DD}, V_{SS}, and V_{DDSPD}.

3. Motivation to Combine

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Harris with the FBDIMM Standards with a reasonable expectation of success because Harris states that its Figure 1A may be a "fully buffered DIMM" (FBDIMM or FBD). Pet. 16. Petitioner contends that a person of ordinary skill in the art would have understood that this type of DIMM is standardized in JEDEC's FBDIMM Standards and thus, would naturally look to them for more details about the "fully buffered DIMM" that Harris describes as compatible with his on-board voltage regulator module (VRM). *Id.*

Patent Owner does not dispute Petitioner's motivation to combine Harris and the FBDIMM Standards. *See* Prelim. Resp.

Petitioner has sufficiently shown that a person of ordinary skill in the art would have combined Harris and the FBDIMM Standards since Harris states that its memory module may include fully buffered DIMMs (FBDs). Ex. 1023 ¶ 9. We agree that one of ordinary skill in the art would have recognized this as a standard and looked to the FBDIMM Standards for information concerning the voltage values standardized for use in an FBDIMM. Ex. 1027, 83; Ex. 1028, 9. Petitioner has shown sufficiently that one of ordinary skill in the art would have combined Harris and the FBDIMM Standards with a reasonable expectation of success.

4. Analysis of Independent Claim 1

a) Limitation 1.a: "A memory module comprising:"

Petitioner asserts that Harris's memory module 100A in Figure 1A or memory module 306-1 in Figure 3 corresponds to the claimed "memory module." Pet. 19–20 (citing Ex. 1023 ¶¶ 9, 17, 20, Figs. 1A, 3; Ex., 1003 ¶¶ 217–223; Ex. 1028, 38). Harris does indeed disclose a memory module with multiple memory devices such as DRAMs 110-1 to 110-N in Figure 1A or 306-1, for example, in Figure 3.

Patent Owner does not specifically respond to Petitioner's contention for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Harris teaches the preamble for purposes of institution.[2]

> *b) Limitation 1.b: "a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system"*

Petitioner asserts that Harris and the FBDIMM Standards disclose this limitation. Pet. 20–25. Petitioner contends that Harris and the FBDIMM standard disclose printed circuit boards (PCBs). Pet. 20 (citing Ex. 1023 ¶ 13, Figs. 1A, 3). Petitioner also contends that a PCB may be referred to as a 'memory board' or 'raw card.' *Id.* at 20–21 (citing Ex. 1023 ¶ 9, Ex. 1028, 10, 38, 84; Ex. 1003 ¶¶ 223–225).

As for the PCB "having an interface configured to fit into a corresponding slot connector of a host system," Petitioner notes that Harris's Figure 3 shows that each memory module 306-1 to 306-M includes an edge connection for fitting into a corresponding slot of a host system. Pet. 21 (citing Ex. 1023 ¶¶ 2, 12, 13, 19, Figs. 3, 4; Ex. 1028, 38, 84; Ex. 1003 ¶¶ 227–228).

Petitioner further contends that Harris, consistent with the FBDIMM Standards, discloses that the edge connections are "configured to couple power, data, address and control signals between the memory module and

[2] Neither party argues whether the preamble limits claim 1. Although we find that the evidence supports that the prior art teaches the preamble, we make no determination at this stage of the proceeding that the preamble of claim 1 is limiting.

the host system." Pet. 21–25. Petitioner contends that the power signal corresponds to Harris's voltage 104 in Figure 1A. *Id.* at 21 (citing Ex. 1023 ¶¶ 10, 12, 19). Petitioner contends that Harris's buffer 112 in Figure 1A is called "AMB" (Advanced Memory Buffer) in the FBDIMM Standards. Pet. 23–24. Petitioner indicates that Harris's buffer 112 receives data, address, and control signals via memory controller interface 114 and transmits these signals to DRAMs 110-1 to 110-N in Figure 1A. Pet. 22–25 (citing Ex. 1023 ¶ 9 ("buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of memory devices 110-1 through 110-N"). In addition, Petitioner argues that the FBDIMM Standards indicate that buffer AMB receives data signals DQ0–DQ63; address signals A0–A15; and control signals RAS, CAS, WE, CS, etc. Pet. 22–23 (citing Ex. 1028, 13).

Patent Owner argues that Petitioner has not made a *prima facie* case that Harris discloses a memory module having a PCB interface that receives power from the host system. Prelim. Resp. 14–20. Harris states, however, that DRAM devices may be "powered from system board or main board voltage sources." Ex. 1023 ¶ 2. Harris also discloses that "external voltage sources may comprise any combination of *known* or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages." Ex. 1023 ¶ 14 (emphasis added). Patent Owner does not argue that voltage supplied by a host system is not a "known" voltage supply as referenced by Harris. Furthermore, Petitioner indicates that the FBDIMM Standards show that the buffer AMB may be connected to a host, suggesting that the FBDIMM may derive its power from the host. Pet. 24 (showing figure at Ex. 1027, 4). These facts point to the conclusion that Harris's

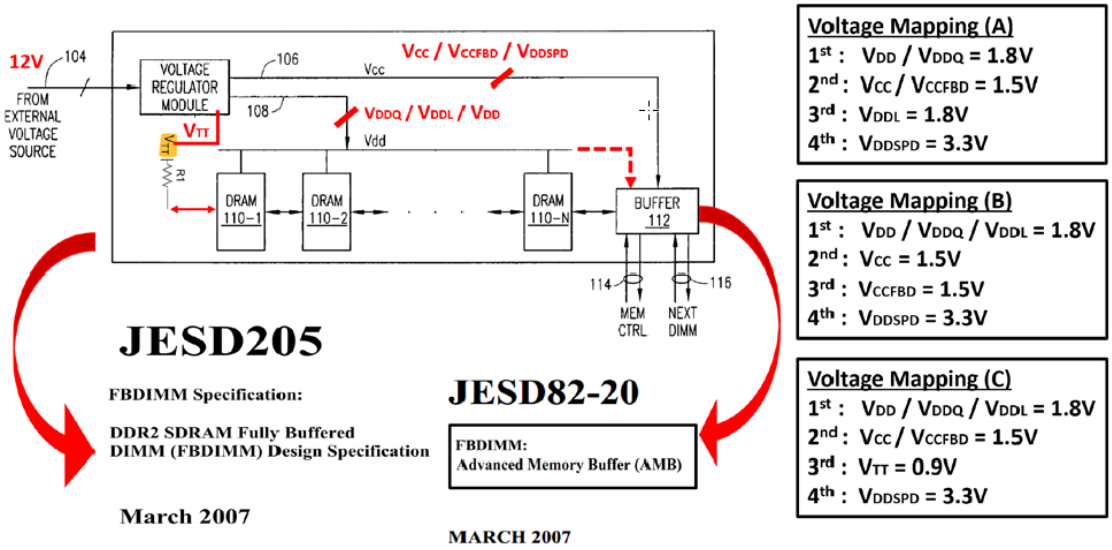
external voltage source may be the host system notwithstanding Patent Owner's arguments to the contrary.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches this limitation for purposes of institution.

> *c) Limitations 1.c to 1.f: "a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude;"*

Petitioner contends that Harris and the FBDIMM Standards disclose limitations 1.c to 1.f. Pet. 26–31. Petitioner relies on an annotated version of Harris's Figure 1A, shown below.

Ground 1: Harris with JEDEC's FBDIMM Standards



Above is Harris's Figure 1A annotated with information one would have obtained from the FBDIMM Standards according to Petitioner. Pet. 26 (citing Pet. 14–19; Ex. 1003 ¶¶ 232–243, 250–257, 262–276, 281–287). Specifically, the above figure shows voltage mappings A, B, and C of four voltages specified by Harris and the FBDIMM Standards. Petitioner contends the voltage range described in Harris (0.5V–3.5V) is the same range as the voltages described in the FBDIMM Standards. *Id.* at 27 (citing Ex. 1023 ¶ 9). Petitioner contends the voltages would be "regulated" because Harris indicates "tightly regulated power" is a problem to be solved, and proposes "at least one on-board voltage regulator" that is "capable of generating tightly-controlled voltage levels" as the solution. *Id.* at 28 (citing Ex. 1023 ¶¶ 2, 3, 9–11; Ex. 1003 ¶ 234).

Petitioner further contends that Harris teaches using "buck converters" to provide the four regulated voltages. *Id.* (citing Ex. 1003 ¶¶ 236, 237, 252, 264, 286). Specifically, Petitioner contends that Harris discloses "replacing [the prior art] power supply interface pins with as few as six +12V pins (from an external voltage source)" and then using "a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels" to provide each needed on-board regulated voltage. *Id.* (alteration by Petitioner; emphasis omitted; citing Ex. 1023 ¶¶ 10, 12). Petitioner contends that a "buck converter" was a conventional device for implementing such a "voltage-reducing switching converter." *Id.* (emphasis omitted; citing Ex. 1030, 2:41–43). Although the claim states that a converter circuit generates the fourth voltage, Petitioner notes that a buck converter would be an obvious way to implement a converter circuit. *Id.* at 28, n.2. Petitioner further contends a buck converter would have been an obvious way to step

down a higher input voltage of 12V to a lower output voltage of 3.5V or less, and that there would have been a reasonable expectation of success because buck converters were well-known switching devices commonly used to step down the voltage between input and output, as had long been taught in textbooks. *Id.* at 28–29 (citing Ex. 1003 ¶¶ 146–149, 236–237; Ex. 1058, 3, 5, 12–16; Ex. 1032, 161, 164; Ex. 1024, Fig. 6; Ex. 1050, 1:21).

Petitioner further notes that "buck converters" were well-known as a highly-efficient way to step down voltages without generating excess heat or requiring large cooling devices, providing further motivation to use buck converters. *Id.* at 29–30 (citing Ex. 1003 ¶ 237; Ex. 1040, 1, 23, 24, Figs. 22–25; Ex. 1041, 1, 13; Ex. 1048, 3; Ex. 1058, 5; Ex. 1059, 5:23–30; Ex. 1062, 11; Ex. 1064 ¶ 101).

Petitioner further contends that it would have been obvious to use at least four converters in Harris given the need for four different voltages (e.g., 0.9V, 1.5V, 1.8V, 3.3V) in the FBDIMM Standards. *Id.* at 30 (citing Pet. 14–19). Petitioner asserts that it would have been obvious to use four converters because the voltages at the same level in Petitioner's voltage mappings A and B are described as separate voltages with separate pins that are separately controllable in the FBDIMM Standards. *Id.* at 30–31 (citing Ex. 1028, 17–20, 30–32; Ex. 1026, 9; Ex. 1003 ¶¶ 242, 256; Ex. 1062, 13).

Patent Owner argues that Harris requires at most two or three buck converters to provide the voltages needed and thus, does not disclose the four claimed converters. Prelim. Resp. 20–25. Specifically, Patent Owner contends that Harris discloses a single converter generating two regulated voltages, so Harris does not disclose four converters as claimed. Prelim. Resp. 21–22. Petitioner showed sufficiently that the FBDIMM Standards

mentioned in Harris call for at least four voltages, and that given Harris's teaching of a converter, it would have been obvious to one of ordinary skill in the art to use multiple converters, including well-known buck converters, to generate the four voltages needed. Pet. 26–31. Patent Owner's argument thus, appears to be an attack on Harris alone without considering what the combination of Harris and the FBDIMM Standards would have suggested to a person of ordinary skill in the art. "Non-obviousness cannot be established by attacking references individually where the rejection is based upon the teachings of a combination of references." *In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (citing *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

Patent Owner further contends that Petitioner has not made out a case to use two or more buck converters to provide voltages having the same level. Prelim. Resp. 25–29. Petitioner explained sufficiently, however, that the FBDIMM Standards identify V_{DD}, V_{DDQ} and V_{DDL} as well as V_{CC} and V_{CCFBD} as separate voltages of the same level with separate pins that can be turned on and off independently of one another. Pet. 30–31. Petitioner contends this provides independence for the power supplies with improved stability and flexibility for power management. *Id.* at 31. Petitioner also relies on voltage mapping C (Pet. 27) which has different voltage levels for the four voltages used, so Patent Owner's argument, even if correct, would not negate Petitioner's showing with respect to this voltage mapping.

Patent Owner contends that Petitioner did not make the case that a person of ordinary skill in the art would have used a third buck converter, as opposed to a linear regulator, to provide termination voltage V_{TT}. Prelim. Resp. 29–33. Petitioner explained sufficiently that "buck converters" were

well-known as a highly-efficient way to step down voltages without generating excess heat or requiring large cooling devices, providing further motivation to use buck converters. Pet. 29–30.

Patent Owner contends that Petitioner does not explain why a person of ordinary skill in the art would have generated the voltage V_{TT} on the module as opposed to obtaining V_{TT} from interface pins. Prelim. Resp. 29–30. Patent Owner similarly argues that Petitioner does not explain why one of ordinary skill in the art would have generated V_{DDSPD} on the module instead of continuing to use the regulated voltage supplied via the V_{DDSPD} pin on a standard DIMM. Prelim. Resp. 33–34.

Harris's Figure 1A shows that the voltages V_{cc} and V_{dd} are generated on the module. On this record, we agree with Petitioner that it would logically follow to generate V_{TT} on the module using the same voltage regulator module 102 as used to generate voltages V_{cc} and V_{dd}. *See* Pet. 15–19. In addition, "when there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 421. Here, there are only two options—generate the voltage V_{TT} on the module, as Petitioner indicates, or obtain the voltage V_{TT} from interface pins. Petitioner's choice of the former of the two options does not negate its showing of obviousness.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches limitations 1.c to 1.f of claim 1 for purposes of institution.

> *d) Limitation 1.g: "a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:"*

Petitioner asserts that Harris discloses a "a plurality of components coupled to the PCB" including a Buffer and DRAMs shown in Harris's Figure 3, and a Serial Presence Detect (SPD) and resistors. Pet. 31 (citing Pet. 14–19; Ex. 1003 ¶¶ 288–90, 293–297). Petitioner further contends that these components are each coupled to at least one or more of the second, third and fourth regulated voltages. *Id.*

Patent Owner does not dispute that the combination of Harris and the FBDIMM Standards discloses this feature. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMMs Standards teaches this limitation for purposes of institution.

> *e) Limitation 1.h: "a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and"*

Petitioner asserts that Harris discloses that the plurality of components includes a plurality of DDR DRAM devices 110-1 to 110-N as shown in Harris's Figure 1A and DRAM devices 312-1 to 312-8 for each of the memory modules shown in Harris's Figure 3. Pet. 32 (citing Ex. 1023 ¶¶ 9, 11, Figs. 1A, 3; Ex. 1003 ¶¶ 298–303). Petitioner contends that a person of ordinary skill in the art would have known that according to the JEDEC standards, DDR memory devices are "synchronous" DRAM devices. *Id.* (citing Ex. 1028, 9; Ex. 1045, cover; Ex. 1026, cover; Ex. 1046, cover).

Patent Owner does not dispute that the combination of Harris and the FBDIMM Standards discloses this feature. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMMs Standards teaches this limitation for purposes of institution.

f) Limitation 1.i.1: "at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices"

Petitioner contends that the "first circuit" corresponds to Harris's buffer 112 as shown in Harris's Figure 1A, as well as the buffer of memory module 306-1 in Harris's Figure 3. Pet. 32–34 (citing Pet. 20–25; Ex. 1003 ¶¶ 304–317). Petitioner contends that Harris's buffers are coupled to receive data, address, and control signals via memory controller interface 114 across edge connections, and transmits them to DRAMs 110-1 to 110-N or DRAMs 312-1 to 312-8. *Id.*

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches this limitation for purposes of institution.

g) Limitation 1.i.2: "the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge

connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices"

Petitioner relies on the same showing for limitation 1.i.2 as for limitation 1.i.1. Pet. 32–34.

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches this limitation for purposes of institution.

h) Limitation 1.i.3: "the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage"

Petitioner contends that Harris with the FBDIMM standards discloses this limitation. Pet. 34–35 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 318–323). Specifically, Petitioner contends that Harris's buffer 112 in Figure 1A is coupled to "the second regulated voltage" (e.g., V_{CC} or V_{CCFBD}=1.5V) and "the fourth regulated voltage" (e.g., V_{DDSPD}=3.3V). *Id.*

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards teaches this limitation for purposes of institution.

i) Limitation 1.i.4: "wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes."

Petitioner contends that "one of the second and fourth voltages" (e.g., 1.5V) "is less than a second one of the second and fourth voltages" (e.g. 3.3V). Pet. 35 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 324–327).

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards teaches this limitation for purposes of institution.

j) Determination for Claim 1

Petitioner shows sufficiently that one of ordinary skill in the art would have had reason to combine Harris and the FBDIMM Standards with a reasonable expectation of success in arriving at claim 1. Furthermore, Petitioner has shown sufficiently that the combination of Harris and the FBDIMM Standards teaches each limitation of claim 1. Accordingly, Petitioner has established a reasonable likelihood to prevail in showing that claim 1 is unpatentable as obvious over the combination of Harris and the FBDIMM Standards.

5. Claims 2, 3, 8, 14, and 15

Claim 2 depends from claim 1 and recites "wherein the first and third buck converters are further configured to operate as a dual buck converter." EX. 1001, 38:53–55. Petitioner contends that the combination of Harris and the FBDIMM Standards discloses this limitation. Pet. 35–40. Specifically, Petitioner contends that at the time there were many commercially available

products that could output two regulated voltages using buck converters, and thus, it would have been obvious to implement two or more of the regulated voltages such as the "first" and "third" voltages as a "dual buck converter" to reduce the number of integrated circuits, pins, and interconnections on the module, therefore simplifying the design. Pet. 36 (Ex. 1003 ¶ 338). Petitioner contends that commercially available devices included the Murata MPD4S014S dual buck converter (EX. 1042, 6; Ex. 1048, 1–2; Ex. 1058, 5), the Texas Instruments TPS51020 Dual Step-Down Controller (Ex. 1040, 1, 11) and the Fairchild Semiconductor FAN5026 Dual-Output PWM Controller" (Ex. 1041, 1, 2, 9). *See* Pet. 36–40.

Patent Owner presents no argument specific to claim 2. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards renders claim 2 obvious for purposes of institution.

Claims 3 depends from claim 1 and recites "wherein the first voltage amplitude is 1.8 volts." Ex. 1001, 38:56–57. Petitioner contends that the combination of Harris and the FBDIMM Standards discloses this limitation. Pet. 41 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 348–353).

Patent Owner presents no argument specific to claim 3. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards renders claim 3 obvious for purposes of institution.

Claim 8 depends from claim 1 and recites

> the plurality of components further comprising:
> one or more registers coupled to one of the first, second, third and fourth regulated voltages, the one or more registers configured to register, in response to a clock, the first plurality of address and control signals, wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.

Ex. 1001, 39:9–19.

Petitioner contends the combination of Harris and the FBDIMM Standards discloses claim 8. Pet. 41–46. Specifically, Petitioner contends that Harris's buffer 112 is a component that has registers to register incoming signals and output them according to a "clock" signal, as shown in Harris's Figures 1A and 3. *Id.* at 41. Petitioner contends Harris's buffer 112 is coupled to the voltage V_{CC} or V_{CCFBD} as the "second regulated voltage." *Id.* (citing Pet. 14–19, 27). Petitioner contends Harris discloses "buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data" which a person of ordinary skill in the art would understand involves registers for registering the address, control, and data signals in response to a "clock" signal. *Id.* at 42 (citing Pet. 22–25; Ex. 1023 ¶¶ 9, 17, Fig. 3; Ex. 1003 ¶¶ 400–402; Ex. 1027, 19) (emphasis omitted).

Petitioner further contends that the combination of Harris and the FBDIMM Standards discloses an S3 sleep mode that selectively switches off the second voltage to turn off the power to the one or more registers while the DRAMs remain powered on to refresh data in the DRAMs. Pet. 45 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 410–411, 414–420; Ex. 1012 ¶ 9; Ex. 1027, 21, 39).

Patent Owner presents no arguments specific to claim 8. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards renders obvious claim 8 for purposes of institution.

Claim 14 depends from claim 8 and recites

> wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.

Ex. 1001, 39:40–45.

Petitioner contends that when the S3 sleep mode ends, normal DRAM transactions begin again and the second voltage which powers the input/output registers switches on and the registers output the registered address and control signals to the SDRAM devices. Pet. 46 (citing Ex. 1027, 25; Ex. 1003 ¶¶ 462–466).

Patent Owner presents no argument specific to claim 14. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards renders claim 14 obvious for purposes of institution.

Claim 15 depends from claim 1 and recites

> the plurality of components further comprising:
> a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated

> circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.

Ex. 1001, 39:46–52.

Petitioner contends that the combination of Harris and the FBDIMM Standards discloses claim 15. Pet. 47–50. Specifically, Petitioner contends logic in Harris's buffer includes an integrated circuit, as does its serial presence detect (SPD), including non-volatile memory. Pet. 47 (citing Ex. 1027, 25; Ex. 1003 ¶¶ 435–437, 468–476). Petitioner further contends the logic element includes discrete elements such as resistors and capacitors to terminate voltages for Harris's buffer. *Id.* Petitioner asserts that the S3 sleep mode of the FBDIMM Standards requires S3 Recovery Configuration Registers. *Id.* According to Petitioner, an FBDIMM like Harris's memory module will store configuration information in non-volatile memory before entering into S3 sleep mode. *Id.* (citing Ex. 1027, 25, 95, 96, 141). Petitioner further contends that a person of ordinary skill in the art would have understood that the "non-volatile memory" can be implemented in the SPD device separate from the integrated circuit implements the AMB (Advanced Memory Buffer) where the SPD is used to store configuration information in the non-volatile memory. *Id.* at 48–49 (citing Ex. 1023 ¶ 19; Ex. 1027, 117; Ex. 1028, 13; Ex. 1066, 26:64–27:4; Ex. 1067, p.1-1; Ex. 1003 ¶ 436). Petitioner further contends a person of ordinary skill in the art would have understood that the logic element includes discrete electrical elements such as resistors and capacitors, as taught by the FBDIMM Standards. *Id.* at 49–50 (citing Ex. 1003 ¶ 475; Ex. 1023 ¶ 9, Fig. 1A; Ex. 1028, 13, 42–45).

Patent Owner presents no argument specific to claim 15. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards renders claim 15 obvious for purposes of institution.

6. Claim 23

Claim 23 is an independent claim. Ex. 1001, 40:50–41:21. Petitioner contends that the limitations of claim 23 are substantially identical to earlier limitations, and are thus obvious for the reasons stated above. Pet. 50–51.

Patent Owner presents no additional argument for claim 23 other than arguments previously discussed. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Harris in combination with the FBDIMM Standards renders obvious claim 23.

7. Determination for Ground 1

Petitioner has shown a reasonable likelihood to prevail in showing unpatentability of claims 1–3, 8, 14, 15, and 23 as obvious over the combination of Harris and the FBDIMM Standards for the reasons explained.

D. Ground 2: Obviousness Over Harris, the FBDIMM Standards, and Amidi

Petitioner contends that claims 1–30 of the '918 patent would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi. Pet. 41–70. For the reasons that follow, we are persuaded that the evidence, including Dr. Wolfe's testimony, sufficiently supports Petitioner's

arguments and, therefore, establishes a reasonable likelihood of prevailing with respect to this ground at this stage of the proceeding.

1. Amidi (Ex. 1024)

Amidi was filed on October 25, 2006, issued on May 25, 2010, and is titled "Clock and Power Fault Detection for Memory Modules." Ex. 1024, codes (22), (45), (54). Petitioner contends Amidi is prior art under § 102(e). Pet. 12.

Amidi's Figure 5 is reproduced below.

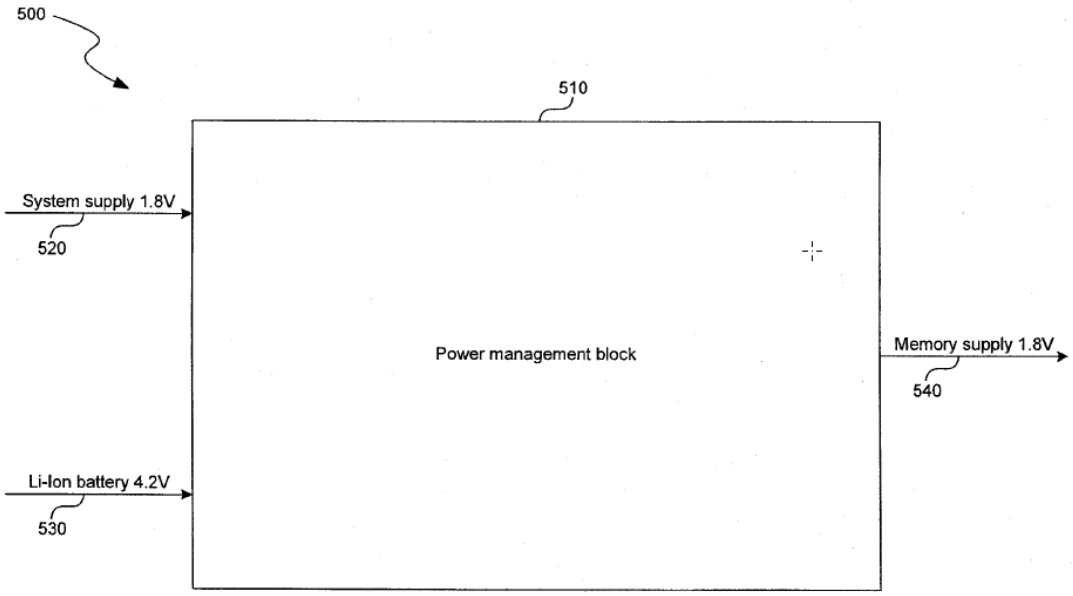


FIG. 5

Amidi's Figure 5 above illustrates a power management block 510 that receives an incoming system supply 520, and incoming battery supply 530, and generates an outgoing memory power supply 540 which is stabilized in the face of disruptions to the system supply 520 using the battery supply 530. Ex. 1024, 4:14–22, 8:23–36, Figs. 5, 14; Ex. 1003 ¶¶ 131–132.

2. Motivation to Combine

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Harris and the FBDIMM Standards with Amidi with a reasonable expectation of success. Pet. 52. Specifically, Petitioner contends that Harris recognizes concerns with power reliability and proposes the use of a redundant power source. *Id.* (citing Ex. 1023 ¶¶ 12–14, 16, Figs. 1B, 2). Petitioner notes that Amidi teaches a redundant power source (a battery on the memory module) for maintaining data during power disruption. *Id.* at 52–53 (citing Ex. 1024, code (57), 1:28–35, 2:6–26, 4:14–60, Figs. 5–6; Ex. 1003 ¶¶ 171–177). Petitioner further notes that Amidi's power management block could be modified easily to work with Harris's FBDIMM memory module by changing the system supply 520 and memory supply 540 to 12V as taught by Harris. *Id.* at 53 (citing Ex. 1024, Figs. 5, 6; Ex. 1023 ¶ 12; Ex. 1003 ¶¶ 173–174). Petitioner contends that to a person of ordinary skill in the art it would have been obvious to use the 12V external supply stepped-down with a buck converter to a 5V supply for charging Amidi's battery, and that Amidi's battery voltage would be stepped-up with a boost converter to the 12V level used by Harris's memory module. *Id.* at 53–54 (citing Ex. 1024, Fig. 6 (620); Ex. 1003 ¶¶ 171–172). Petitioner contends that Amidi discloses that its power management block uses "buck" converters to step-down voltages as needed, and "boost" converters to step-up voltages as needed, as had long been taught in textbooks. *Id.* at 54 (citing Ex. 1024, 4:27–32, 4:38–40, Figs. 5, 6; Ex. 1058, 3; Ex. 1032, 161). Petitioner further contends that Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory

module and the FBDIMM standards, such that a person of ordinary skill in the art would have been motivated to combine their teachings. *Id.* at 54–56.

Petitioner contends that the combination of Harris, the FBDIMM Standards, and Amidi would result in the following configuration and voltage mappings:

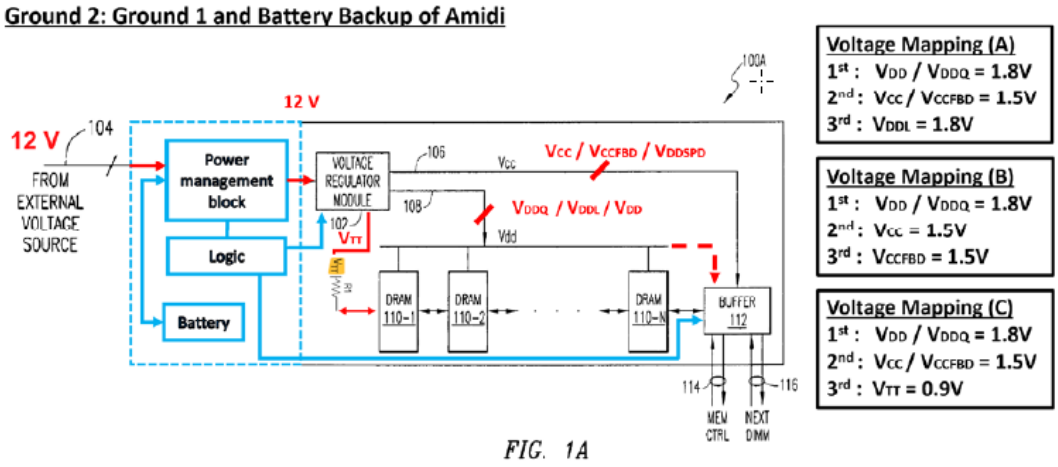


FIG. 1A

Pet. 56. Above, Petitioner has annotated Harris's Figure 1A to show features added from the teachings of the FBDIMM Standards (red) and features added from the teachings of Amidi (blue).

Patent Owner argues that Harris provides alternate voltage sources to power a memory module in the event of a power interruption, so Harris already provides a solution for the alleged problem that Amidi addresses. Prelim. Resp. 35–39. Harris does not appear to describe, however, switching to an alternate voltage source in response to power loss, nor does it explicitly mention a battery as an alternate voltage source, whereas Amidi does. Ex. 1024, code (57). Thus, Patent Owner's argument does not undermine Petitioner's motivation to combine the references.

Patent Owner also argues that "Petitioner has entirely ignored the issue of whether the essential parts of Amidi it seeks to apply to the

combination would even fit onto Harris's circuit board, particularly where Petitioner has already proposed to add additional converters." Prelim. Resp. 38–39. Patent Owner's declarant, Dr. Sunil Khatri, states that space on the board to fit all of the components that Patent Owner proposes would have been a concern. Ex. 2001 ¶¶ 78, n.3, 79. As explained above, however, Petitioner argues that one of ordinary skill would have had reasonable expectation of success in making the combination and supports its argument with credible testimony from Dr. Wolfe who explains how one of ordinary skill would have been able to incorporate Amidi's functionality in the FBDIMM memory module of Harris and that such modification would have been well within the level of skill at the time. Ex. 1003 ¶¶ 170–179.

Accordingly, we determine Petitioner has adequately shown that one of ordinary skill in the art would have been motivated to combine Harris, the FBDIMM Standards, and Amidi with a reasonable expectation of success.

3. Claims 1–3, 8, 14, 15, and 23

We agree with Petitioner that the addition of Amidi does not negate Petitioner's showing with respect to the previous ground. Pet. 56, 66–67 (citing Ex. 1003 ¶¶ 215–353, 412–413, 467–476, 557–597). Accordingly, Petitioner has shown a reasonable likelihood to prevail in demonstrating claims 1–3, 8, 14, 15, and 23 are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi for the reasons stated in the previous ground.

4. Claims 16–22 and 30

Claims 16–22 recite a "pre-regulated input voltage." Ex. 1001, 39:61, 42:23. Petitioner identifies at least two meanings for this claim term, one meaning within pre-determined limits and the other meaning the voltage

must be pre-regulated on the memory board itself. Pet. 73. For purposes of this decision, we interpret "pre-regulated voltage" to mean that the voltage is regulated before conversion to a stepped up or down level. *See* Ex. 1001, code (57), 28:53–58, Fig. 16 (1110, 1112). Patent Owner further argues that Amidi does not disclose a "pre-regulated voltage" but offers no interpretation for the term. Prelim. Resp. 39–40. We invite development of the record at trial to explain the meaning of "pre-regulated input voltage." In any case, we find Petitioner's showing of obviousness with respect to these claims sufficient for institution.

5. Claims 5–7, 9–13, 16–22, and 24–27

Claims 5–7, 9–13, 16–22 and 24–27 recite, or depend from a claim that recites, that the voltage monitor circuit generates the trigger signal in response to the input voltage being greater than a predetermined threshold voltage. Ex. 1001, 38:61–67, 40:7–13, 41:22–27, 42:21–26. Claims 5–7, 9–13, 16, 17, 20–22, and 24 require generation of a trigger signal, and we determine that Petitioner sufficiently shows for institution that these claims would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi. Claims 18, 19, 25, and 26 require that the trigger signal causes a controller to execute a write operation. We determine that Petitioner's showing of obviousness is sufficient for these claims for purposes of institution, although we invite further explanation of the parties' views of the combination of Harris, the FBDIMM Standards, and Amidi at trial.

6. Determination for Ground 2

Petitioner has demonstrated that a person of ordinary skill in the art would have had reason to combine Harris, the FBDIMM Standards, and

Amidi with a reasonable expectation of success. Petitioner has also demonstrated that all of the limitations of at least one claim in this ground are taught or suggested by the combination. Accordingly, under this ground, Petitioner has demonstrated a reasonable likelihood to prevail in showing unpatentability of at least one claim of the '918 patent as obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

E. Ground 3: Obviousness over Harris, the FBDIMM Standards, Amidi, and Hajeck

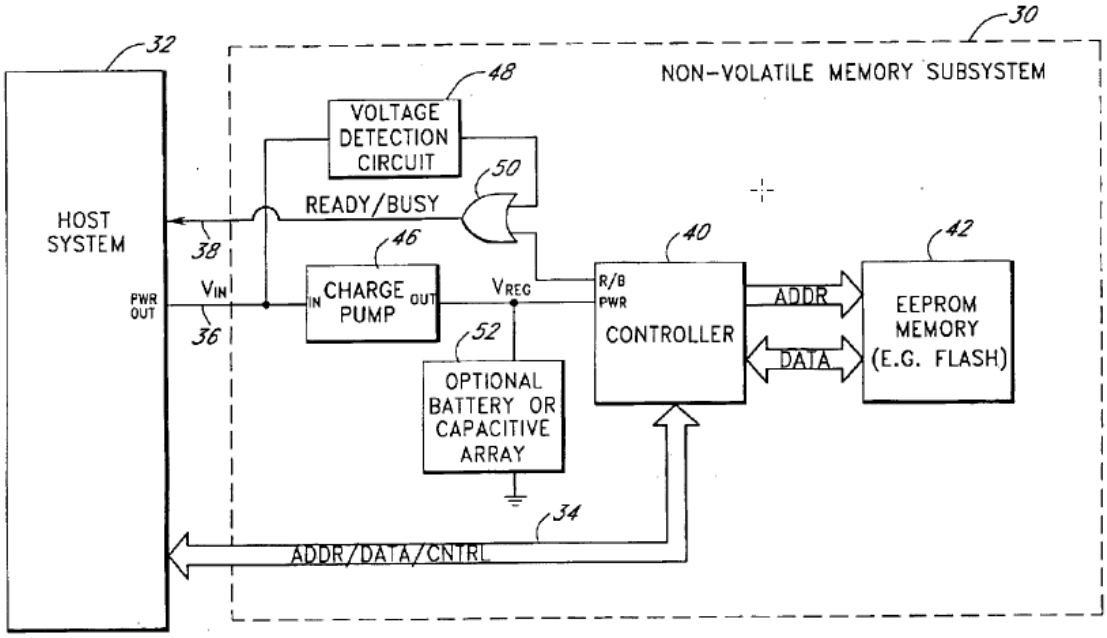
Petitioner contends claims 1–30 would have been obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck. Pet. 75–77.

1. Hajeck (Ex. 1038)

Hajeck is titled "Storage Subsystem with Embedded Circuit for Protecting Against Anomalies in Power Signal from Host." Ex. 1001, code (54). Hajeck issued as U.S. Patent No. 6,856,556 B1 on February 15, 2005. Petitioner contends Hajeck is prior art under § 102(b). Pet. 12.

Hajeck seeks to protect storage subsystems from damage and data loss caused by irregularities in a power signal provided by a host. Ex. 1038, 1:10–13. Specifically, Hajeck seeks to prevent data loss due to loss of power from a host system, and to prevent power surges or spikes from damaging circuitry of the storage subsystem. *Id.* at 1:15–31.

Hajeck's Figure 1 is reproduced below.



In Hajeck's Figure 1, non-volatile memory subsystem 30 receives power from host system 32 at charge pump 46 which supplies regulated voltage to controller 40. *Id.* at 2:64–67. In the event of a power surge or spike, charge pump 46 protects controller 40 from damage. *Id.* at 3:12–16. In the event of a voltage drop, charge pump 46 with battery and capacitive array 52 provides sustained voltage to controller 40. *Id.* at 2:60–63, 3:10–13. Voltage detection circuit 48 detects anomalies in the input voltage, including undervoltage and overvoltage conditions, and generates a "busy" signal provided to the host system 32 to block the host system from performing write operations to the storage subsystem. *Id.* at 1:64–67, 3:30–43.

2. Motivation to Combine

Petitioner contends that one of ordinary skill in the art would have been motivated to combine Hajeck with Harris, the FBDIMM Standards, and Amidi because one would have appreciated the desirability of switching to backup power in both undervoltage and overvoltage conditions. Pet.

75–76. Hajeck teaches to use a backup power supply, such as a charge pump, battery, or capacitive array, in response to power loss from the host system to complete outstanding operations, and to use the charge pump to protect the controller from surges or spikes in the power supply. *See, e.g.*, Ex. 1038, code (57), 1:53–61. To the extent that Hajeck and the other prior art would have been used to back up data to prevent its loss during a power interruption, one would have been able to make the combination to arrive at the claims requiring a write operation to non-volatile memory in response to a signal. *See, e.g.*, claims 11 and 12. We invite further development of the record on the reasons to combine Hajeck with Harris, the FBDIMM Standards, and Amidi. For purposes of institution, Petitioner shows sufficiently that a person of ordinary skill in the art would have combined Harris, the FMDIMM Standards, Amidi, and Hajeck with a reasonable expectation of success.

3. Claims 1–3, 8, 14, 15, and 23

We are not aware of any reason why the addition of Hajeck would negate Petitioner's showing with respect to the previous grounds which incorporate Harris, the FBDIMM Standards, and Amidi. Accordingly, Petitioner has shown a reasonable likelihood to prevail in demonstrating claims 1–3, 8, 14, 15, and 23 are unpatentable as obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck for the reasons stated.

4. Determination for Ground 3

Petitioner demonstrates a reasonable likelihood to prevail in showing that at least one claim of the '918 patent is unpatentable as obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck.

F. Ground 4: Obviousness over Spiers and Amidi

Petitioner contends that claims 1–30 are obvious over the combination of Spiers and Amidi. Pet. 77–127.

1. Spiers (Ex. 1025)

Spiers is titled "Non-Volatile Memory Backup for Network Storage System." Ex. 1025, code (54). Spiers was filed on October 12, 2004, and published on April 13, 2006 as U.S. Patent Pub. No. 2006/0080515 A1. *Id.* at codes (10), (43). Petitioner contends that Spiers is prior art under § 102(b). Pet. 13.

Spiers's Figure 4 is reproduced below.

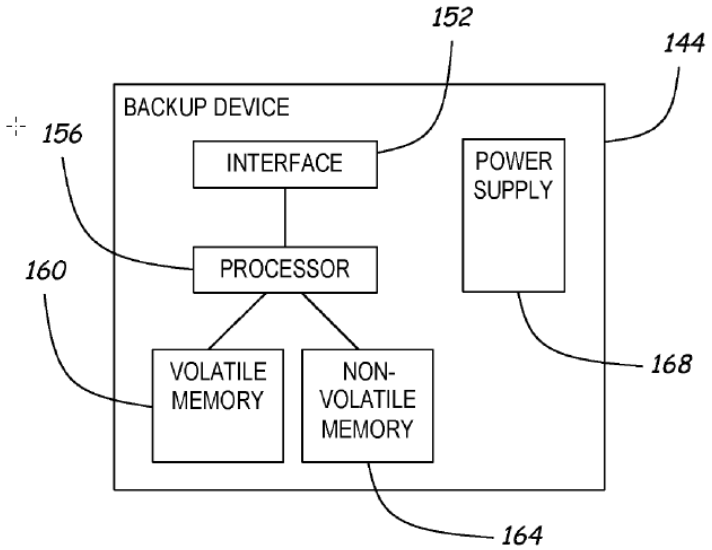


FIG.4

Spiers's Figure 4 above shows backup device 144. Ex. 1025 ¶ 36. Backup device 144 comprises an interface 152, backup device processor 156, volatile memory 160, non-volatile memory 164, and power supply 168. *Id.* Interface 152 communicates with storage controller 132 (not shown). *Id.* Interface 152 connects to processor 156 which controls operations within backup device 144. *Id.* Processor 156 connects to volatile memory 160 and

non-volatile memory 164. *Id.* Volatile memory 160 may be an SDRAM used to store data from storage controller 132 during typical write operations. *Id.* Non-volatile memory 164 may be flash memory and is used in the event of a power failure detection. *Id.* Upon detecting a power failure, processor 156 switches backup device 144 to power supply 168 (capacitors or batteries) and moves data in volatile memory 160 to non-volatile memory 164. *Id.*

2. Motivation to Combine

Petitioner contends that one of ordinary skill in the art would have been motivated to combine Spiers and Amidi. Pet. 78–81. Petitioner contends one would have used Amidi to learn implementation details, such as specific type of SDRAM devices and voltage regulators, useful for Spiers. *Id.* at 78–79 (citing Ex. 1003 ¶¶ 196–200). Petitioner contends while Spiers teaches SDRAM devices, Amidi specifically discloses DDR SDRAM devices. *Id.* at 79 (citing Ex. 1024, claims 4–5). Petitioner contends a person of ordinary skill in the art would have been motivated to implement Spiers with commercially available DDR2 or DDR3 SDRAMs powered according to relevant JEDEC standards with a reasonable expectation of success when using such well-known, standardized technology. *Id.* (citing Ex. 1003 ¶¶ 198–200).

Patent Owner argues that Spiers only mentions two voltage regulators, and that Petitioner provides no reason why a person of ordinary skill in the art would have used DDR2 or DDR3 devices, which require more than two regulated voltages, instead of the SDR SDRAM devices specified by Spiers. Prelim. Resp. 42–43. Petitioner contends that Amidi provides a reason to use DDR2 or DDR3 SDRAMs powered according to relevant JEDEC

standards. Pet. 79 (citing Ex. 1003 ¶¶ 198–200). Patent Owner contends that Spiers's writes to SDRAM occur with every system write, and that Petitioner makes no showing that DDR2/DDR3 devices would have been used for such a high write-to-read ratio application. Prelim. Resp. 41 (Ex. 2001 ¶ 90; Ex. 1025 ¶¶ 34, 36, 40, 41, Figs. 11, 12).

Patent Owner's evidence does not establish that DDR2 or DDR3 devices would not work in Petitioner's combination, only that they would be sub-optimal in that application. On the current record, we cannot determine that such a solution would be sufficiently sub-optimal that one of ordinary skill in the art not have pursued it, but instead would have looked to some other unidentified solution. *See also Novartis Pharms. Corp. v. West-Ward Pharms. Int'l Ltd.*, 923 F.3d 1051, 1059 (Fed. Cir. 2019) (noting that an obviousness showing "does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention." (quoting *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004))).

Patent Owner also argues that SDRAM devices could operate at or above the data rates of a PCI interface used by Spiers, so replacing Spiers's SDRAM devices with faster DDR2 or DDR3 would not bring about a gain in data rate or justify the added expense of additional voltage regulators to accommodate DDR2/DDR3 devices. Prelim. Resp. 41–42 (citing Ex. 2001 ¶¶ 90–92).

Patent Owner's argument assumes that Spiers is limited to a PCI interface, but a PCI backup device is described as one embodiment in Spiers. Ex. 1025 ¶ 19. Spiers also discloses an "interface 152" in more general terms, which does not appear limited to a PCI interface. *Id.* ¶ 36. Patent

Owner has not shown that the interfaces that one of ordinary skill in the art would have considered to use in light of Spiers would not have been able to accommodate faster DDR2/DDR3 devices. Accordingly, we disagree with this argument on the record as thus far developed.

Petitioner has shown sufficiently that one of ordinary skill in the art would have combined Spiers and Amidi with reasonable expectation of success.

3. Claim 1

a) Limitation 1.a: "A memory module comprising:"

Petitioner contends that Spiers discloses the preamble of claim 1. Pet. 82. Petitioner contends that Spiers's backup device 144 corresponds to the claimed "memory module." *Id.* at 77. Spiers's backup module 144 has both volatile memory (SDRAMs 190) and non-volatile memory (NAND flash 194). *Id.* (citing Ex. 1025 ¶¶ 34, 37, Figs. 3, 5; Ex. 1003 ¶¶ 643–646).

Patent Owner does not specifically respond to these arguments. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Spiers teaches the preamble for purposes of institution.

b) Limitation 1.b: "a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system"

Petitioner contends that Spiers discloses this limitation. Pet. 83–85. Petitioner asserts that Spiers's PCI card of backup device 144 corresponds to "a printed circuit board (PCB)." *Id.* at 83. Petitioner contends that Spiers's

PCI card has an interface configured to fit into the slot connector of a host system, and including a plurality of edge connections. *Id.* (citing Ex. 1025, Fig. 5). Petitioner contends these edge connections are configured to couple power, data, address, and control signals between the memory module and host system. *Id.* at 84 (citing Ex. 1025 ¶¶ 37, 39, 54; Ex. 1031, 1, 7, 21–25, 146–150; Ex. 1003 ¶¶ 652–654).

Patent Owner submits no argument specific to this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Spiers teaches this limitation for purposes of institution.

> *c) Limitations 1.c to 1.f: "a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude;"*

Petitioner contends that the combination of Spiers and Amidi discloses these limitations. Pet. 86–93. Petitioner provides the following figure to explain how the combination teaches these limitations:

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

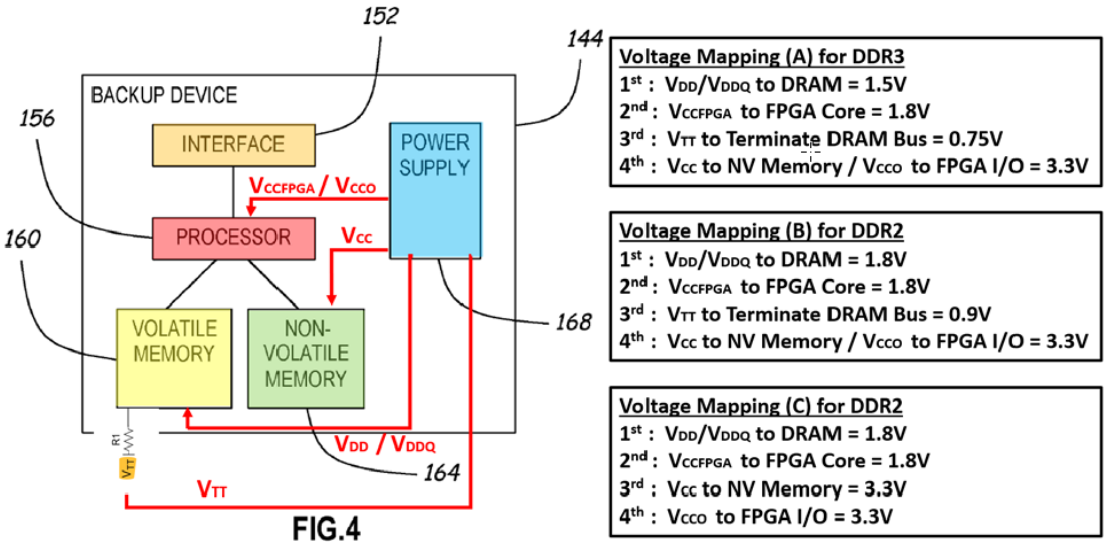


FIG.4

Pet. 86. The above figure shows Petitioner's view of what a person of ordinary skill in the art would have understood from the combined teachings of Spiers and Amidi in light of the JEDEC standards that would have been known to those of ordinary skill in the art. Pet. 86 (citing Ex. 1003 ¶¶ 655–700). Specifically, Petitioner indicates correspondences between the first, second, third and fourth regulated voltages and those used in Spiers's backup device 144 shown as voltage mappings A, B, and C. *Id.*

Petitioner contends that Spiers's PCI card uses a +5V power supply of the PCI bus to power components of the card, including the SDRAM devices (190, 218) required power supply voltages such as V_{DD}/V_{DDQ} ("first regulated voltage") with amplitudes depending upon the specific DRAM type (DDR2, DDR3, etc.). *Id.* at 87. Petitioner contends that a person of ordinary skill in the art would have recognized that terminal voltage V_{TT} ("third regulated voltage" in voltage mappings A and B) is required for communicating with DRAM devices. *Id.* at 87–88 (citing Ex. 1003 ¶¶ 680–684; Ex. 1025 ¶¶ 37, 46, Fig. 9; Ex. 1028, 68). Petitioner also

contends that Spiers's voltage regulator 206 provides V_{CCFPGA}=1.8V regulated power ("second regulated voltage") to the FGPA core. Pet. 88 (citing Ex. 1025 ¶ 37, Fig. 5; Ex. 1003 ¶¶ 670–673). Petitioner further contends that a person of ordinary skill in the art would have understood that different FPGAs have different voltage requirements for the FPGA core. Pet. 88 (citing Ex. 1042, 2).

Petitioner also contends that Spiers discloses a voltage regulator 184 configured to step down a 5V backup voltage to a 3.3V output voltage used to transfer data from the volatile to non-volatile memories 194, and that a person of ordinary skill in the art would have understood that the 3.3V can be used as V_{CC} power to the non-volatile memories ("third regulated voltage" in mapping C and "fourth regulated voltage" in mappings A and B). *Id.* at 88–89 (citing Ex. 1025, Fig. 5; Ex. 1049, 38; ; Ex. 1003 ¶¶ 685–687, 691–698).

Petitioner further contends a person of ordinary skill in the art would have understood that a converter circuit such as voltage regulator 184 or similar, is configured to provide regulated voltage V_{CCO} of 3.3V ("fourth regulated voltage" in mapping C, "third regulated voltage" in mappings A and B) to an interface of processor 198 to transfer data to and from the non-volatile memories 194. Pet. 89 (citing Ex. 1042, 2, 16; Ex. 1003 ¶¶ 691–700).

Petitioner further contends it would have been obvious to use buck converters to generate these regulated voltages to achieve high efficiency, reliability, and flexible power conversion. Pet. 90 (citing Pet. 29–31; Ex. 1025, Fig. 14 (step 752); Ex. 1062, 11; Ex. 1003 ¶¶ 662–666). Petitioner contends that buck converters powering SDRAM and FPGA

devices from higher voltage sources were well known and commercially available at the time, as disclosed by Amidi. *Id.* at 90–91 (citing Ex. 1024, 4:38–41, Fig. 6 (640)). Petitioner further contends that there were commercially available buck converters to implement the proposed combination. *Id.* at 91–93 (citing Ex. 1047, 1:28–32, 2:47–55, 5:56–59, 7:6–14; Ex. 1042, 1, 2, 9; Ex. 1042, 16, Ex. 1048, 1, 2; Ex. 1058, 5).

Patent Owner argues that Spiers describes its memory devices as SDR SDRAMs, not DDR2 or DDR3 devices. Prelim. Resp. 42–46. Patent Owner further contends that Petitioner has not shown why one would have replaced Spiers's SDRAM with DDR2 or DDR3 devices. *Id.* at 47–53. Petitioner contends, however, that Amidi specifically discloses DDR SDRAM devices. Pet. 79 (citing Ex. 1024, claims 4–5). Petitioner further contends the person of ordinary skill in the art would have been familiar with the JEDEC standards for DDR2 and DDR3 devices, which specify the four or more voltages required for those memory devices. *Id.* Pet. 79 (citing Ex. 1026; Ex. 1046).

Patent Owner contends that Petitioner did not provide any evidence why one would need to use V_{TT} in the DDR2 or DDR3 standards. Prelim. Resp. 53–56. Even if Patent Owner is correct, Petitioner did not rely solely on V_{TT} as the third regulated voltage. *See* Pet. 86.

Patent Owner argues there is no evidence that one would have generated V_{TT} using a buck converter. Prelim. Resp. 53–56. Petitioner explained that the reason for using a buck converter for regulated voltages comes from Amidi. *See* Pet. 91 (citing Ex. 1024, 4:38–41, Fig. 6 (640)).

Patent Owner further argues that Petitioner provided no reason for equipping Spiers with multiple 1.8V regulators. Prelim. Resp. 59–60.

Petitioner explained that the JEDEC standards provide for separate pins with the same voltage levels, and that certain voltages should be isolated and separately controlled to provide independence, stability, and flexibility for power management. Pet. 30–31.

Patent Owner further argues there are other ways to generate regulated voltages than providing a buck converter for each voltage level, and Petitioner did not show why one would not have pursued these other options. Prelim. Resp. 60–69. Petitioner did explain, however, that using a buck converter for each regulated voltage would "achieve high efficiency, reliability, and flexible power conversion." Pet. 90 (citing Pet. 29–31; Ex. 1025, Fig. 14; Ex. 1062, 11; Ex. 1003 ¶¶ 662–666).

Petitioner has shown sufficiently for institution that the combination of Spiers and Amidi teaches this claim limitation.

> *d) Limitation 1.g: "a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:"*

Petitioner contends that Spiers's DRAM, FPGA/processor, resistors, and non-volatile memory are components coupled to the PCI card, which are each coupled to at least one of three regulated voltages. Pet. 94 (citing Pet. 78–81; Ex. 1003 ¶¶ 701–713).

Patent Owner provides no argument specific to this limitation. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

e) Limitation h: "a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and"

Petitioner asserts that Spiers discloses SDRAMs 190 that may be implemented as DDR2 or DDR3 devices. Pet. 94 (citing Pet. 32, 78–81; Ex. 1003 ¶¶ 714–718).

Patent Owner provides no argument specific to this limitation. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

f) Limitation 1.i.1: "at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices,"

Petitioner contends that the "at least one circuit" corresponds to Spiers FPGA processor 198 coupled to the SDRAM devices 190, 218 and to the PCI interface 172 for data, address and control signals. Pet. 95.

Patent Owner does not specifically respond to Petitioner's contention. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

g) Limitation 1.i.2: "the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices,"

Petitioner contends that Spiers's FPGA processor 198 receives read and write commands from the PCI interface 172 and outputs address and control signals on DDR SDRAM interface between 198 and 190 to the

SDRAM devices. Pet. 95–98 (citing Ex. 1025 ¶¶ 37, 39, 44–46, Figs. 5, 9; Ex. 1031, 1, 7, 21, 146–149, Ex. 1003 ¶¶ 724–729).

Patent Owner does not specifically address Petitioner's contention for this limitation. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

h) Limitation 1.i.3: "the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,"

Petitioner contends that Spiers's FPGA processor is coupled to both the second regulated voltage (V_{CCFPGA}=1.8V) and the fourth regulated voltage (V_{CCO}=3.3V). Pet. 98–99 (citing Pet. 78–81; Ex. 1003 ¶¶ 730–734).

Patent Owner does not specifically respond to Petitioner's contention. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

i) Limitation 1.i.4: "wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes"

Petitioner contends that Spiers discloses that one of the second and fourth amplitudes (e.g., 1.8V) is less than a second one of the second and fourth amplitudes (e.g., 3.3V). Pet. 99 (citing Pet. 78–81, 87; Ex. 1003 ¶¶ 735–738).

Patent Owner does not specifically respond to Petitioner's contention. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

j) Determination for Claim 1

Petitioner shows sufficiently that one of ordinary skill in the art would have had reason to combine Spiers and Amidi with a reasonable expectation of success in arriving at claim 1. Furthermore, Petitioner has shown sufficiently that the combination of Spiers and Amidi teaches each limitation of claim 1. Accordingly, Petitioner has established a reasonable likelihood to prevail in showing that claim 1 is unpatentable as obvious over the combination of Spiers and Amidi.

4. Claims 2–30

We have reviewed Petitioner's contentions for each of claims 2–30. Pet. 99–130. We find them sufficient to disclose the limitations recited in at least claims 2–4, 8, 14, 15, 23, and 28–30.

Patent Owner contends that claim 23 requires a second voltage to be selectively switched on or off, and that Petitioner maps the second voltage as the voltage supply to the processor core. Prelim. Resp. 71 (citing Pet. 99). Patent Owner contends that Petitioner's mapping relates to turning off the supply voltage to the system bus, not the processor core. *Id.* (citing Pet. 114–15). Patent Owner does not explain why turning off the voltage supply on the system bus would not also turn off the power to the processor core. Although Patent Owner further argues that the processor must remain on while backing up data in the SDRAM, Patent Owner does not indicate what language in claim 23 requires the processor core to be switched on during data backup.

Other than these arguments previously addressed, Patent Owner does not present any further argument specific to these claims. *See* Prelim. Resp.

Petitioner has shown sufficiently that the combination of Spiers and Amidi discloses at least one of these claims.

Accordingly, Petitioner has established a reasonable likelihood to prevail in showing at least one of these claims is unpatentable as obvious over the combination of Spiers and Amidi under this ground.

G. Ground 5: Obviousness over Spiers, Amidi, and Hajeck

Petitioner contends that a person of ordinary skill in the art would have combined Hajeck with Spiers and Amidi because Hajeck teaches the importance of detecting both undervoltage and overvoltage conditions to avoid data loss. Pet. 128–29. Hajeck teaches generating a busy signal for a host in response to undervoltage or overvoltage conditions, and also teaches that its charge pump protects its controller from being damaged by spikes and surges in a power signal provided by a host. Ex. 1038, 1:64–67, 3:13–16, 3:30–43.

On this record, Petitioner's showing is sufficient to present a reasonable likelihood that at least one of claims 1–30 is unpatentable as obvious over the combination of Spiers, Amidi, and Hajeck. Pet. 128–30. Also, this ground subsumes the previous one, and there is no persuasive evidence that Hajeck negates Spiers and Amidi, so Petitioner has presented a reasonable likelihood to prevail in showing at least one of claims 1–30 is unpatentable as obvious over the combination of Spiers, Amidi, and Hajeck under this ground.

IV. CONCLUSION

After considering the evidence and arguments presented in the Petition and Preliminary Response, we determine that Petitioner has

established a reasonable likelihood of prevailing on its assertion that at least one claim of the '918 patent is unpatentable. We institute an *inter partes* review on all the challenged claims and all of the grounds presented in the Petition. At this stage of the proceeding, we have not made a final determination as to the patentability of these challenged claims.

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that pursuant to 35 U.S.C. § 314, *inter partes* review is instituted as to the challenged claims of the '918 patent with respect to all grounds of unpatentability presented in the Petition; and

FURTHER ORDERED that *inter partes* review is commenced on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

IPR2022-00996
Patent 11,016,918 B2

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Paper 11
Entered: December 6, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00999
Patent 11,232,054 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and NABEEL U. KHAN, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition (Paper 1, "Pet.") to institute an *inter partes* review of claims 1–30 of U.S. Patent 11,232,054 B2, issued on January 25, 2022 (Ex. 1001, "the '054 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.") to the Petition.

Institution of an *inter partes* review is authorized when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a).

Based on the current record, and for the reasons explained below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one challenged claim, and we institute an *inter partes* review as to all the challenged claims and grounds raised in the Petition.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies Samsung Electronics Co., Ltd. and Samsung Semiconductor, Inc. as the real parties in interest. Pet. 1. Patent Owner identifies itself as the sole real party in interest. Paper 4, 1.

B. Related Matters

The parties advise that the '054 patent is related to *Samsung Electronics Co., Ltd., et al. v. Netlist, Inc.*, IPR2022-00996; *Netlist, Inc. v. Samsung Electronics Co., Ltd., et al.*, Case No. 2-21-cv-00463 (E.D. Tex.); *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, Case No. 1:21-cv-01453 (D. Del.); and U.S. Appl. No. 17/582,797. Pet. 1; Paper 4, 1.

The parties advise that the '054 patent is related to the following legal proceeding, which is no longer pending: *SK hynix Inc. v. Netlist, Inc.*, IPR2017-00692. Pet. 1; Paper 4, 1.

C. The '054 Patent (Ex. 1001)

The '054 patent is titled "Flash-DRAM Hybrid Memory Module." Ex. 1001, code (54). Figure 12 of the '054 patent is reproduced below.

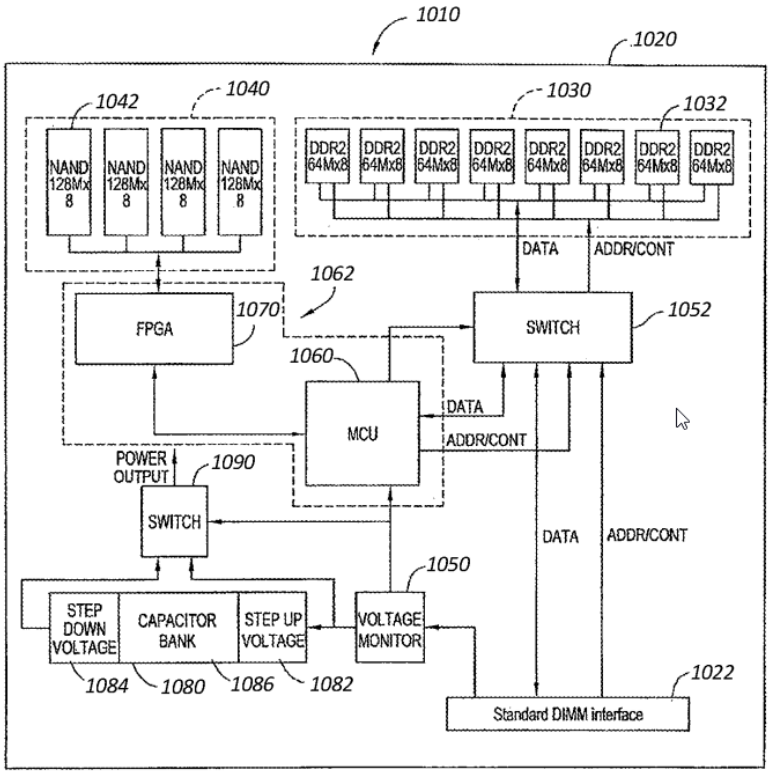


FIG. 12

Figure 12 shows an example memory system 1010 of the '054 patent. *Id.* at 21:14–16. The memory system 1010 includes a volatile memory subsystem 1030, a non-volatile memory subsystem 1040, and a controller 1062 operatively coupled to the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. *Id.* at 21:16–20. Volatile memory 1030 may comprise elements 1032 of two or more dynamic random access memory (DRAM) elements such as double data rate (DDR), DDR2, DDR3, and synchronous DRAM (SDRAM). *Id.* at 22:16–19. Non-volatile memory 1040 may comprise elements 1042 of flash memory elements such as NOR, NAND, ONE-NAND flash and multi-level cell (MLC). *Id.* at 22:35–40. Memory system 1010 may comprise a memory module or printed circuit board 1020. *Id.* at 21:24–26. Memory system 1010 has an interface 1022

for power voltage, data, address, and control signal transfer between memory system 1010 and a host system. *Id.* at 22:3–6.

Controller 1062 may include microcontroller unit 1060 and FPGA logic 1070, either as separate devices or integrated together. *Id.* at 24:35–37, 23:19–22, Fig. 14. Microcontroller 1060 may transfer data between the volatile memory 1030 and non-volatile memory 1040. *Id.* at 24:35–41. Logic element 1070 provides signal level translation and address translation between the volatile memory and the non-volatile memory. *Id.* at 24:45–56.

When the system is operating normally, controller 1062 controls switch 1052 to decouple the volatile memory 1030 from controller 1062 and the non-volatile memory 1040 (the '054 patent refers to this as the "first state"). *Id.* at 24:60–25:7. In response to a power interruption, for example, controller 1062 controls switch 1052 to couple the volatile memory 1030 to itself and non-volatile memory 1040, and transfers data from the volatile memory to the non-volatile memory to prevent its loss (the '054 patent refers to this as the "second state"). *Id.* at 25:9–20.

Memory system 1010 may comprise a voltage monitor 1050 to monitor voltage supplied from the host system via interface 1022. *Id.* at 25:8–10. When the voltage monitor 1050 detects a low voltage condition, the voltage monitor transmits a signal to the controller 1062 to indicate the detected condition. *Id.* at 25:11–15.

Power may be supplied from a first power supply (e.g. a system power supply) when the memory system 1010 is in the first state and from a second power supply 1080 when the memory system 1010 is in the second state. *Id.* at 25:54–58. Second power supply 1080 may comprise step-up transformer

1082, step-down transformer 1084, and capacitor bank 1086 with one or more capacitors. *Id.* at 26:3–13.

The memory system 1010 further has a third state in which controller 1062 is decoupled from the volatile memory system 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). *Id.* at 25:62–66. The third power supply may provide power to volatile memory subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred. *Id.* at 25:66–26:3.

Figure 16 of the '054 patent is reproduced below.

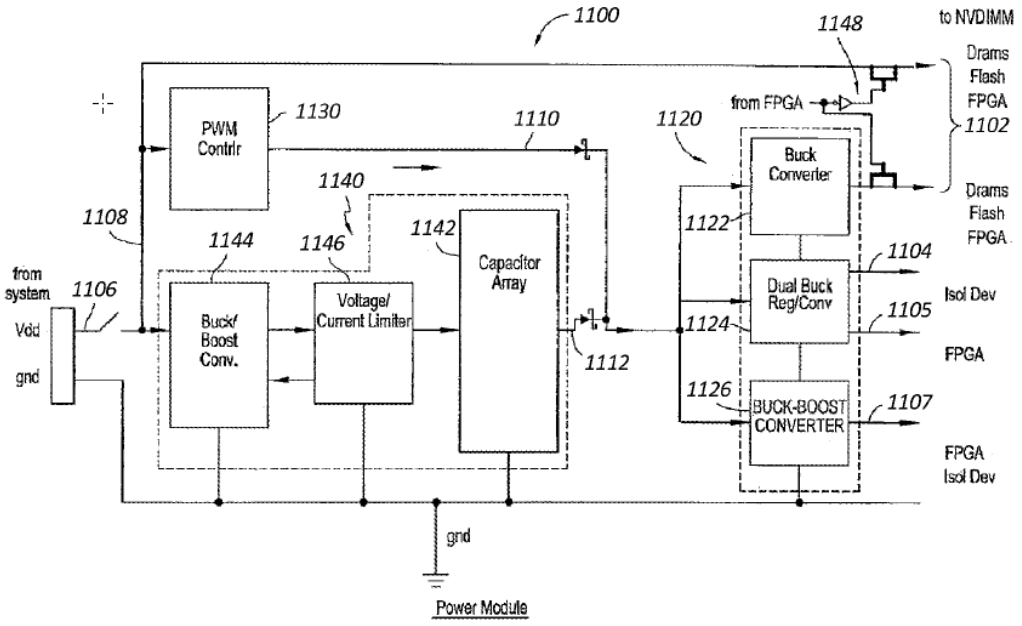


FIG. 16

Figure 16 shows power module 1100 of memory system 1010. *Id.* at 27:59–61. Power module 1100 comprises conversion element 1120, first power element 1130, and second power element 1140. *Id.* at 28:7–15, 28:20–22. Conversion element 1120 comprises buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 generating respective

voltages 1102, 1104, 1105, 1107 from the outputs of the first and second power elements 1130, 1140. *Id.* at 28:62–67. The first power element 1130 may comprise a pulse-width modulation power controller generating voltage 1110 from voltages 1106, 1108. *Id.* at 28:13–15. Second power element 1140 may comprise capacitor array 1142, buck-boost converter 1144 receiving voltages 1106, 1108 and adjusting the voltage for charging the capacitor array, and voltage/current limiter 1146, which limits charge current to the capacitor array and stops charging the capacitor array 1142 when it reaches a certain charge voltage. *Id.* at 28:62–67. Power module 1100 provides power to components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition. *Id.* at 27:61–65.

Specifically, in a first state, first voltage 1102 is provided to memory system 1010 from input 1106 and fourth voltage 1102 is provided to conversion element 1120 from the first power element 1130. *Id.* at 28:27–31. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120. *Id.* at 28:31–34. In the third state, the fifth voltage is provided to conversion element 1120 from second power element 1140 and the first voltage 1104 is provided to memory system 1010 from conversion element 1120. *Id.* at 28:34–38. Transition from the first state to the second state may occur when power module 1100 detects a power failure is about to occur, and transition from the second state to the third state may occur when it detects a power failure has occurred. *Id.* at 28:39–47.

D. Illustrative Claim

Of the challenged claims, claims 1, 16, and 24 are independent. Independent claim 1, reproduced below with brackets noting Petitioner's identifiers, is illustrative of the claimed subject matter.

> 1. [1.a] A memory module comprising:
>
> [1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
>
> [1.c] a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;
>
> [1.d] [1.d.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages, [1.d.2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and [1.d.3] a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections, [1.d.4] wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and [1.d.5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.

Ex. 1001, 38:19–44.

E. Evidence

Petitioner relies on the following references (*see* Pet. 3, 9–14), as well as the Declaration of Dr. Andrew Wolfe (Ex. 1003).

Reference	Exhibit No.	Patent/Printed Publication
Harris	1023	U.S. Patent Pub. No. 2006/0174140 A1 to Harris, published August 3, 2006
Amidi	1024	U.S. Patent No. 7,724,604 B2, issued May 25, 2010
Spiers	1025	U.S. Patent Pub. No. 2006/0080515 A1, published Apr. 13, 2006
FBDIMM Standards	1027, 1028	JESD82-20 and JESD205 standards published March 2007
Hajeck	1038	U.S. Patent No. 6,856,556 B1 to Hajeck, issued February 15, 2005

F. Prior Art and Asserted Grounds

Petitioner asserts that claims 1–30 are unpatentable on the following Grounds (Pet. 4):

Claims Challenged	35 U.S.C. §	References
1–3, 15	103(a)	Harris, FBDIMM Standards
1–30	103(a)	Harris, FBDIMM Standards, Amidi
1–30	103(a)	Harris, FBDIMM Standards, Amidi, Hajeck
1–30	103(a)	Spiers, Amidi
1–30	103(a)	Spiers, Amidi, Hajeck

III. ANALYSIS OF CHALLENGED GROUNDS

We turn now to Petitioner's asserted grounds of unpatentability and Patent Owner's arguments in its Preliminary Response to determine whether Petitioner has met the threshold standard of 35 U.S.C. § 314(a).

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

A patent claim "is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR*, 550 U.S. at 418. An obviousness determination requires finding "both 'that a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted); *see also KSR*, 550 U.S. at 418. Further, an assertion of obviousness "cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR*, 550 U.S. at 418; *In re NuVasive, Inc.*, 842 F.3d 1376, 1383 (Fed. Cir. 2016) (a finding of a motivation to combine "must be supported by a 'reasoned explanation'").

"In an [*inter partes* review], the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable." *Harmonic*, 815 F.3d at 1363 (citing 35 U.S.C. § 312(a)(3)); *see also Intelligent Bio-Sys.*, 821 F.3d at 1369 ("It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'" (quoting 35 U.S.C. § 312(a)(3))). Therefore, to prevail in an *inter partes* review, Petitioner must explain how the proposed combinations of prior art would have rendered the challenged claims unpatentable. At this preliminary stage, we determine whether the information presented in the Petition shows there is a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims would have been obvious over the proposed combinations of prior art.

A. Level of Ordinary Skill in the Art

Petitioner asserts a person of ordinary skill in the art "would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field." Pet. 7–8 (citing Ex. 1003 ¶ 61). Petitioner contends that additional training can substitute for educational or research experience, and vice versa. *Id.* at 8. Petitioner asserts that such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a

computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. *Id.* Petitioner further contends that such "a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers." *Id.* Petitioner further asserts that such "a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry." *Id.*

In the Preliminary Response, Patent Owner applies the level of ordinary skill in the art proposed by Petitioner. Prelim. Resp. 7.

Among the factors that may be considered in determining the level of ordinary skill in the art are the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962–63 (Fed. Cir. 1986)). The evidence presented mostly applies to the educational level of workers in the field, but also touches upon other factors as well. We find Petitioner's proposal is consistent with the level of ordinary skill in the art reflected by the '054 patent and the prior art of record, and, therefore, we adopt Petitioner's proposed level of ordinary skill in the art, with the exception of the open-ended language "at least," for purposes of this Decision.

B. Claim Construction

We construe each claim "in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent," the same standard used to construe the claim in a civil action. 37 C.F.R. § 42.100(b).

Petitioner contends that "no express constructions are needed for this proceeding" but notes that Patent Owner has broadly interpreted some claim terms for purposes of infringement even though a narrower interpretation may be more reasonable. Pet. 8–9 (citing Ex. 1071, 39–46; Ex. 1073, 55–62). Petitioner further contends it is not necessary to determine whether claim terms are governed by § 112, 6th paragraph because at least one of the prior art combinations matches the disclosure of the '054 patent. *Id.* at 9.

At this stage in the proceeding, we need only construe the claims to the extent necessary to determine whether to institute *inter partes* review. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). We determine that, at this stage of this proceeding, there is no need to expressly construe these claim terms in order to determine whether or not to institute review because the parties do not dispute the claimed terms' meanings, and their ordinary and customary meanings suffice for our analysis. However, we do invite the parties to construe the term "pre-regulated voltage" at trial for reasons explained in Section III.E.11, *infra*.

C. Patent Owner's Preliminary Arguments

Patent Owner argues that Petitioner makes conclusory statements and then cites to pages in Dr. Wolfe's declaration (Ex. 1003) without explanation, improperly incorporating several hundred pages of additional briefing. Prelim. Resp. 14 (citing Pet. 57–58, 68–70, 110–112, 123–125; *Cisco Systems, Inc. v. C-Cation Techs., LLC*, IPR2014-00454, Paper 12 (PTAB Aug. 29, 2014) (informative); 37 C.F.R. § 42.6(a)(3)). Petitioner argues that we should reject these alleged improper attempts to incorporate by reference Dr. Wolfe's testimony. *Id.*

In our analysis below, we will determine for ourselves whether the Petition adequately supports the ground and the weight to be accorded the declarant's testimony.

Patent Owner also takes issue with Petitioner's assertion that elements 7b–7c of claim 7 are similar to elements 5b–5c of claim 5. Prelim. Resp. 14–15. Specifically, Patent Owner contends claim 5 pertains to performing a write operation in response to an undervoltage condition whereas claim 7 pertains to an overvoltage condition and Petitioner's cross-reference allegedly provides no analysis why a write operation would be conducted in response to an overvoltage condition. *Id.* at 15. We address Patent Owner's argument in Section III.E.6, *infra*.

D. Ground 1: Obviousness Over Harris and FBDIMM Standards

Petitioner contends claims 1–3 and 15 would have been obvious over the combination of Harris and FBDIMM Standards and relies on the Declaration of Dr. Andrew Wolfe (Ex. 1003) in support. Pet. 14–40. For the reasons that follow, we are persuaded that the evidence, including Dr. Wolfe's testimony, sufficiently supports Petitioner's arguments and,

therefore, establishes a reasonable likelihood of prevailing with respect to this ground at this stage of the proceeding.

1. Harris (Ex. 1023)

Harris is titled "Voltage Distribution System and Method for a Memory Assembly." Ex. 1023, code (54). Harris was published as U.S. Patent Pub. No. 2006/0174140 A1 on August 3, 2006. Petitioner contends Harris is prior art under § 102(a). Pet. 9.

Harris's Figure 1A is reproduced below.

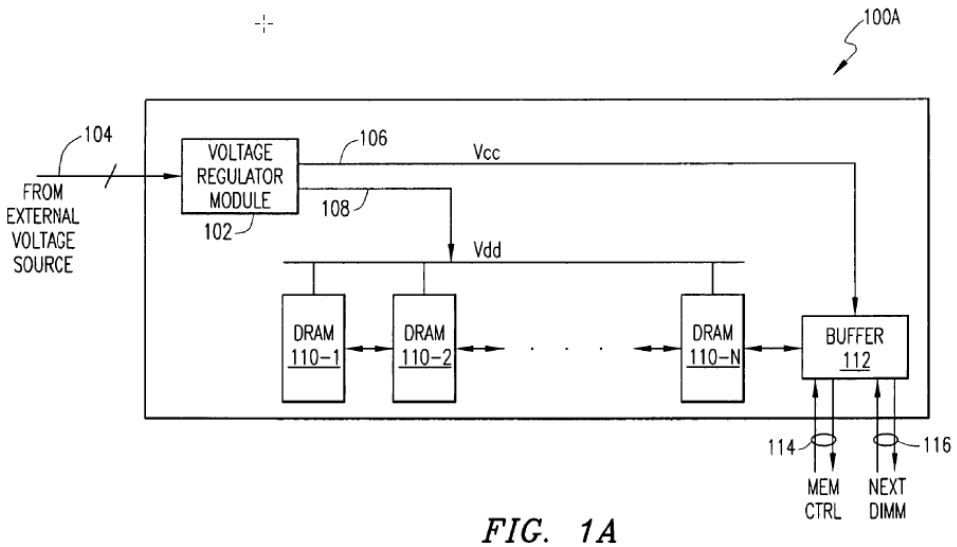


FIG. 1A

As shown in Figure 1A, Harris discloses a memory module 100A including on-board regulator 102 for converting an externally supplied voltage 104 to appropriate local voltage levels 106 (V_{cc}), 108 (V_{dd}), such as 0.5V to 3.5V. Ex. 1023, code (57), ¶¶ 9–10. Voltage 106 is supplied to buffer/logic component 112 which may be connected to a memory controller via interface 114 and daisy-chained with other memory assemblies via interface 116. *Id.* ¶ 9. Voltage 108 powers memory devices 110-1 to 110-N. *Id.* The memory module 100A may be a Dual In-Line Memory Modules (DIMM) wherein each of the memory devices 100-1 to 100-N comprises a Double

Data Rate (DDR), DDR2, or DDR3 device. *Id.* The memory module 100A may be an unbuffered, registered or fully buffered DIMM. *Id.*

2. FBDIMM Standards (Exs. 1027, 1028)

In March 2007, the Joint Electron Device Engineering Council (JEDEC) published standards for Fully Buffered DIMM (FBDIMM) memory modules titled "JESD82-20" (Ex. 1027) and "JESD205" (Ex. 1028). Ex. 1029 ¶¶ 134–137. Petitioner refers to these standards collectively as the "FBDIMM Standards." Pet. 10. Petitioner contends the FBDIMM Standards are prior art under § 102(a).

The FBDIMM Standards specify voltages for components on the memory module as follows:

Product Family Attributes

DIMM organization	x72 ECC			
DIMM dimensions (nominal)	30.35mm (height) x 133.35mm (width) x 8.2 mm (max thickness) MO-256 variation AB 30.35mm (height) x 133.35mm (width) x 8.8 mm (max thickness) MO-256 variation BB			
Pin count	240			
SDRAMs supported	256Mb, 512Mb, 1Gb, 2Gb, 4Gb			
Capacity	256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB			
Serial PD	Consistent with JC 45			
Supply voltages (nominal)	min	typ	max	
	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})
Buffer Interface	High-speed Differential Point-to-point Link at 1.5 volt			
DRAM Interface	SSTL_18			

Note 1: Approximate DC values, refer to AMB Component Specification for actual DC and AC values and conditions.
Note 2: Vtt range accomodates measurable offset due to complementary CA bus current paths. (See Vtt section)
An Unloaded system should supply Vtt of 0.48*Vdd/0.52*Vdd to Dimm socket

Ex. 1028, 9. The above table shows values for supply voltages including DRAM V_{DD}, AMB V_{CC}, DRAM interface V_{TT}, and V_{DDSPD}. The FBDIMMM Standards further specify the following voltages for various power supplies:

Table 9.2 — Pin Description (Sheet 3 of 3)

Signal	Type	Description
$\overline{\text{RESET}}$		Power Good Reset
Miscellaneous Test		
TEST (4 pins)	NC	Pin for debug and test. Must be floated on DIMM.
TESTLO (5 pins)	A	Pin for debug and test. Must be tied to Ground on DIMM
TESTLO_AB20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
TESTLO_AC20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes
Other Pins		
BFUNC	I	**Buffer Function Bit:** When BFUNC = 0, AMB is used as a regular buffer on FB-DIMM. When BFUNC = 1, AMB is used as either a repeater or a buffer for LAI function. On FB-DIMM, BFUNC is tied to Ground
RFU (18 pins)	NC	**Reserved for Future Use.** Must be floated on DIMM. RFU pins denoted by "a" are reserved for forwarded clocks in future AMB implementations.
Other No Connect Pins		
NC (129 pins)	NC	No Connect pins

Ex. 1027, 83. The table above sets voltage levels for power supplies VCC, VCCFBD, VDD, VSS, and VDDSPD.

3. Motivation to Combine

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Harris with the FBDIMM Standards with a reasonable expectation of success because Harris states that its Figure 1A may be a "fully buffered DIMM" (FBDIMM or FBD). Pet. 16. Petitioner contends that a person of ordinary skill in the art would have understood that this type of DIMM is standardized in JEDEC's FBDIMM Standards and

thus would naturally look to them for more details about the "fully buffered DIMM" that Harris describes as compatible with his on-board voltage regulator module (VRM). *Id.*

Patent Owner does not dispute Petitioner's motivation to combine Harris and the FBDIMM Standards. *See* Prelim. Resp.

Petitioner has sufficiently shown that a person of ordinary skill in the art would have combined Harris and the FBDIMM standards since Harris states that its memory module may include fully buffered DIMMs (FBDs). Ex. 1023 ¶ 9. We agree that one of ordinary skill in the art would have recognized this as a standard and looked to the FBDIMM Standards for information concerning the voltage values standardized for use in an FBDIMM. Ex. 1027, 83; Ex. 1028, 9.

4. Analysis of Independent Claim 1

a) Limitation 1.a: "A memory module comprising:"

Petitioner asserts that Harris's memory module 100A in Figure 1A or memory module 306-1 in Figure 3 corresponds to the claimed "memory module." Pet. 19–20 (citing Ex. 1023 ¶¶ 9, 17, 20, Figs. 1A, 3; Ex., 1003 ¶¶ 217–223; Ex. 1028, 38). Harris does indeed disclose a memory module with multiple memory devices such as DRAMs 110-1 to 110-N in Figure 1A or 306-1 in Figure 3.

Patent Owner does not specifically respond to Petitioner's contention for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Harris teaches the preamble for purposes of institution.[1]

> *b) Limitation 1.b: "a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system"*

Petitioner asserts that Harris and the FBDIMM Standards disclose this limitation. Pet. 20–25. For example, Petitioner notes that Harris discloses that its double-rank DIMMs may be accommodated on both sides of a printed circuit board (PCB). Pet. 20 (citing Ex. 1023 ¶ 13). Petitioner further notes that a PCB may be referred to as a 'memory board' or 'raw card.' *Id.* at 20-21 (citing Ex. 1023 ¶ 9, Ex. 1028, 10, 38, 84; Ex. 1003 ¶¶ 224–226).

As for the PCB "having an interface configured to fit into a corresponding slot connector of a host system," Petitioner notes that Harris's Figure 3 shows that each memory module 306-1 to 306-M includes an edge connection for fitting into a corresponding slot of a host system. Pet. 21 (citing Ex. 1023 ¶¶ 2, 12, 13, 19, Figs. 3, 4; Ex. 1028, 38, 84; Ex. 1003 ¶¶ 227–228).

Petitioner further contends that Harris, consistent with the FBDIMM Standards, discloses that the edge connections are "configured to coupled

[1] Neither party argues whether the preamble limits claim 1. Although we find that the evidence supports that the prior art teaches the preamble, we make no determination at this stage of the proceeding that the preamble of claim 1 is limiting.

power, data, address and control signals between the memory module and the host system." Pet. 21–25. Petitioner contends that the power signal corresponds to Harris's voltage 104 in Figure 1A (Ex. 1023 ¶ 10, 12, 19). Petitioner contends that the Harris's buffer 112 in Figure 1A is called "AMB" (Advanced Memory Buffer) in the FBDIMM Standards. Pet. 22. Petitioner indicates that buffer 112 receives data, address, and control signals via memory controller interface 114 and transmits these signals to DRAMs 110-1 to 110-N in Harris's Figure 1A. Pet. 22–25 (citing Ex. 1023 ¶ 9 ("buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of memory devices 110-1 through 110-N")). In addition, Petitioner argues that the FBDIMM Standards indicate buffer AMB receives data signals DQ0–DQ63; address signals A0–A15; and control signals RAS, CAS, WE, CS, etc. Pet. 22–23 (citing Ex. 1028, 13).

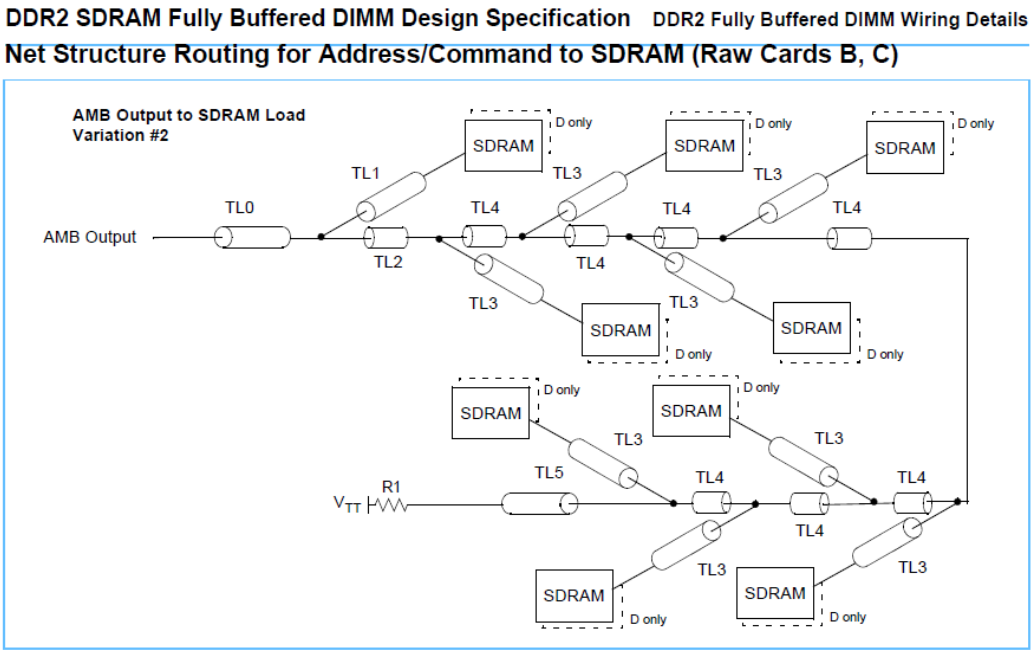
Patent Owner argues that Petitioner has not made a *prima facie* case that Harris discloses a memory module having a PCB interface that receives power from the host system. Prelim. Resp. 15–21. Harris states, however, that DRAM devices may be "powered from system board or main board voltage sources." Ex. 1023 ¶ 2. Harris also discloses that "external voltage sources may comprise any combination of *known* or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages." Ex. 1023 ¶ 14 (emphasis added). Patent Owner does not argue that voltage supplied by a host system is not a 'known' voltage supply as referenced by Harris. Furthermore, Petitioner indicates that the FBDIMM Standards show that the buffer AMB may be connected to a host, suggesting that the FBDIMM may derive its power from the host. Pet. 24 (citing

Ex. 1027, 4). These facts point to the conclusion that Harris's external voltage source may be the host system notwithstanding Patent Owner's arguments to the contrary.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches this limitation for purposes of institution.

> *c) Limitation 1.c: "a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages"*

Petitioner contends that Harris and the FBDIMM Standards disclose limitation 1.c of claim 1 of the '054 patent. Pet. 26–30. Specifically, Petitioner contends that Harris's Voltage Regulator Module 102 corresponds to the claimed "voltage conversion circuit." Pet. 26 (citing Ex. 1023 ¶ 10, Fig. 1A). Petitioner contends that the claimed "at least three regulated voltages" correspond to voltage 106 (V_{cc}) and voltage 108 (V_{dd}) as shown in Harris's Figure 1A, and a third voltage (V_{TT}) which is not actually shown in Harris's Figure but is shown in the FBDIMM Figure below.



Ex. 1028, 68. The figure above shows voltage V_{TT} terminating an array of SDRAM devices via resistor R1.

As to the voltages being "regulated," Petitioner argues Harris discloses that "at least one on-board voltage regulator" is "capable of generating tightly-controlled voltage levels." Pet. 28 (citing Ex. 1023 ¶¶ 2, 3, 9–11; Ex. 1003 ¶ 236).

As to the "at least three buck converters," Petitioner contends that Harris teaches using buck converters to provide the three regulated voltages above. Pet. 28 (citing Ex. 1003 ¶¶ 238–241). Petitioner contends Harris teaches using a "high-frequency switching voltage converter capable of generating tightly-controlled voltage levels" to provide each needed on-board regulated voltage. *Id.* (citing Ex. 1023 ¶¶ 10, 12). Petitioner contends it would have been obvious to use a "buck converter" to convert higher input voltage (e.g., 12V) to the lower output voltage (3.5V or less), and there would have been a reasonable expectation of success because buck

converters were well-known "switching" devices commonly used to step down the voltage between its input and output, as had long been taught in textbooks. *Id.* at 28–29 (citing Ex. 1003 ¶¶ 147–150, 239–241; Ex. 1058, 3, 5, 12–16 (1995 Lenk textbook showing buck, boost, and buck-boost circuits); Ex. 1032, 161 (1995 Mohan textbook showing various step-down (buck) converters); Ex. 1030, 2:32–43, 5:39–44; Ex. 1024, Fig. 6 (Amidi showing DC/DC buck converter; Ex. 1050, 1:21 (identifying buck converters as one of "the most basic building blocks in power electronics"). Petitioner contends buck converters were well-known for their efficiency in generating step down voltages without generating excess heat or requiring large cooling devices. *Id.* at 29 (citing Ex. 1003 ¶ 240; Ex. 1059, 5:23–30; Ex. 1058, 5; Ex. 1040, 1, 23–24; Ex. 1041, 1, 13; Ex. 1048, 3; Ex. 1062, 11; Ex. 1064 ¶ 101). Petitioner contends that it would have been obvious to use at least three converters in Harris given the need for at least three different voltages in the FBDIMM Standards. Pet. 29–30 (citing Ex. 1028, 17–20; Ex. 1026, 2–3, 9; Ex. 1003 ¶¶ 248–249, 255; Ex. 1062, 13; Ex. 1028, 30–32).

Patent Owner argues that Harris requires at most two buck converters to provide the two voltages needed and thus does not disclose "at least three buck converters" as claimed. Prelim. Resp. 24–26. However, as explained, Petitioner relies on Harris for disclosing two voltages V_{cc} and V_{dd}, and the FBDIMM Standards to provide the third voltage V_{TT} such that three buck converters would be needed. *See* Pet. 26–30.

Patent Owner further contends that Petitioner has not made out a case to use two or more buck converters to provide voltages having the same level. Prelim. Resp. 27–30. Petitioner explained, however, that the

FBDIMM standards identify the voltages V_{DD}, V_{DDQ} and V_{DDL} as well as V_{CC} and V_{CCFBD} as separate voltages with separate pins that can be turned on and off separately. Pet. 30.

Patent Owner further contends that Petitioner did not make the case that a person of ordinary skill in the art would have used a third buck converter to provide termination voltage V_{TT}. Prelim. Resp. 30–35. Patent Owner contends that Petitioner does not explain why a person of ordinary skill in the art would have generated the voltage V_{TT} on the module as opposed to obtaining V_{TT} from interface pins. *Id.* at 31. Harris's Figure 1A shows that the voltages V_{cc} and V_{dd} are generated on the module. We agree with Petitioner that it would logically follow to generate V_{TT} on the module using the same voltage regulator module 102 as used to generate voltages V_{cc} and V_{dd}. *See* Pet. 26. In addition, "[when] there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp." *KSR*, 550 U.S. at 421. Here, there are only two options—generate the voltage V_{TT} on the module, as Petitioner indicates, or obtain the voltage V_{TT} from interface pins. Petitioner's choice of the former of two options does not negate its showing of obviousness.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches limitation 1.c of claim 1 for purposes of institution.

> *d) Limitation 1.d.1: "a plurality of components coupled to the PCB, each component of the plurality of*

components coupled to at least one regulated voltage of the at least three regulated voltages"

Petitioner asserts that Harris discloses a "a plurality of components coupled to the PCB" including a Buffer and DRAMs shown in Harris's Figure 3, and a Serial Presence Detect (SPD) and resistors. Pet. 31 (citing Pet. 14–19; Ex. 1003 ¶¶ 261–266). Petitioner further contends that these components are each coupled to at least one regulated voltage of the at least three regulated voltages. *Id.*

Patent Owner does not dispute that the combination of Harris and the FBDIMM Standards discloses this feature. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMMs Standards teaches this limitation for purposes of institution.

e) Limitation 1.d.2: "the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and"

Petitioner asserts that Harris discloses that the plurality of components includes a plurality of DDR DRAM devices 110-1 to 110-N as shown in Harris's Figure 1A and DRAM devices 312-1 to 312-8 for each of the memory modules shown in Harris's Figure 3. Pet. 31–32 (citing Ex. 1023 ¶¶ 9, 11, Figs. 1A, 3; Ex. 1003 ¶¶ 267–271). Petitioner contends that a person of ordinary skill in the art would have known that according to the JEDEC standards, DDR memory devices are "synchronous" DRAM devices. *Id.* at 31–32 (citing Ex. 1028, 9; Ex. 1045, cover; Ex. 1026, cover; Ex. 1046, cover).

Patent Owner does not dispute that the combination of Harris and the FBDIMM Standards discloses this feature. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMMs Standards teaches this limitation for purposes of institution.

f) Limitation 1.d.3: "a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections"

Petitioner contends that the "first circuit" corresponds to buffer 112 as shown in Harris's Figure 1A, as well as the buffer of memory module 306-1 in Harris's Figure 3. Pet. 32–33 (citing Pet. 20–25; Ex. 1003 ¶¶ 272–277). Petitioner contends that Harris's buffers are coupled to receive data, address, and control signals via memory controller interface 114 across edge connections, and transmits them to DRAMs 110-1 to 110-N or DRAMs 312-1 to 312-8.

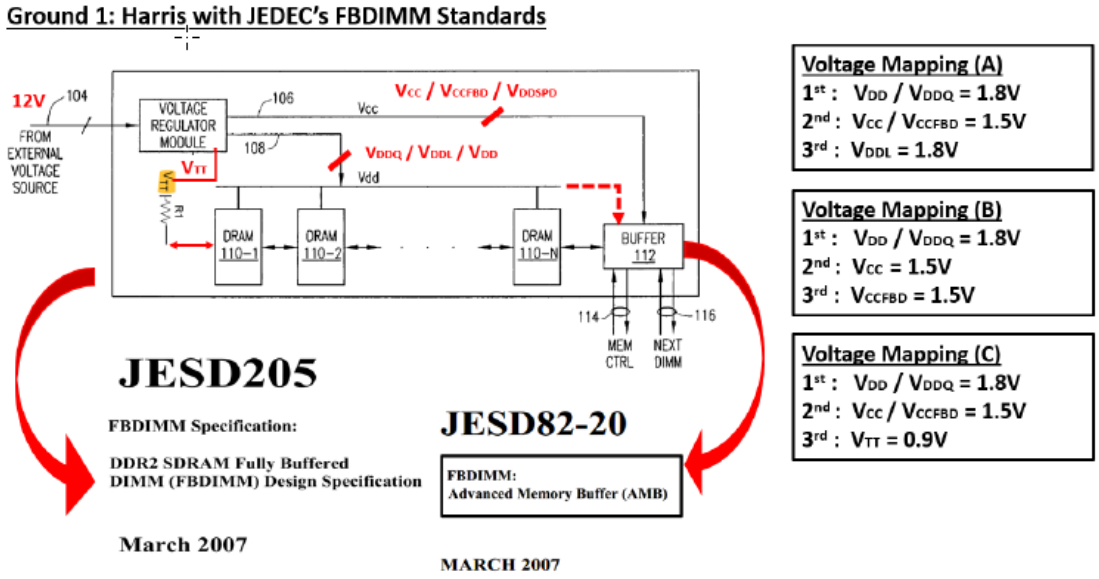
Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris and the FBDIMM Standards teaches this limitation for purposes of institution.

g) Limitation 1.d.4: "wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and"

Petitioner contends that Harris's buffer corresponds to the first circuit and is coupled to "first" (e.g, V_{DD} or V_{DDQ} = 1.8V) and "second" (e.g., V_{CC}

or V_{CCFBD} = 1.5V) "regulated voltages of the at least three regulated voltages." Pet. 33–34 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 278–284). Petitioner provides an annotated version of Harris's Figure 1A shown below.



As shown above, Petitioner fills in Harris's Figure 1A with additional information from the FBDIMM Standards to show that Harris's buffer 112 would be understood by a person of ordinary skill considering the FBDIMM standards to couple to the voltages V_{DD} or V_{DDQ} and V_{CC} or V_{CCFBD}.

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards teaches this limitation for purposes of institution.

h) Limitation 1.d.5: "wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages"

Petitioner contends that Harris with the FBDIMM standards discloses this limitation. Pet. 34 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 285–287). Specifically, Petitioner contends that the SDRAM devices from Harris's Figure 1A are coupled to the first regulated voltage (V_{DD} or V_{DDQ} = 1.8V) of the "at least three regulated voltages." *Id.*

Patent Owner does not specifically respond to Petitioner's contentions for this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that the combination of Harris with the FBDIMM Standards teaches this limitation for purposes of institution.

i) Determination for Claim 1

Petitioner further shows sufficiently that one of ordinary skill in the art would have had reason to combine Harris and the FBDIMM Standards with a reasonable expectation of success in arriving at claim 1. Furthermore, Petitioner has shown sufficiently that the combination of Harris and the FBDIMM Standards teaches each limitation of claim 1. Accordingly, Petitioner has established a reasonable likelihood to prevail in showing that claim 1 is unpatentable as obvious over the combination of Harris and the FBDIMM Standards.

5. Analysis of Dependent Claims

Claim 2 depends from claim 1 and recites "wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude, and wherein a first one of the first and second

voltage amplitudes is less than a second one of the first and second voltage amplitudes." Ex. 1001, 38:45–50. Petitioner contends that, as taught by the FBDIMM Standards, the first voltage amplitude may be 1.8V and the second voltage amplitude may be 1.5V which is less than the first voltage amplitude of 1.8V. Pet. 34 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 288–296).

Claim 3 depends from claim 1 and recites "wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts." Petitioner contends the third regulated voltage is V_{DDL} with a value of 1.8V as shown in the FBDIMM Standards (see previous figure—"voltage mapping (A)"). Pet. 35 (citing Pet. 14–19, 27; Ex. 1003 ¶¶ 297–301).

Claim 15 depends from claim 1 and recites "wherein two of the at least three buck converters are configured to operate as a dual-buck converter." Ex. 1001, 39:59–61. Petitioner contends at the time there were many commercially available products that could output two (or more) regulated voltages using buck converters, and thus "it would be obvious to implement any two of the regulated voltages as a '*dual buck converter*' to reduce the number of integrated circuits, pins, and interconnections on the module, therefore simplifying the design." Pet. 36 (citing Ex. 1003 ¶ 439; *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797–99 (Fed. Cir. 2021)). Petitioner contends that the Murata MPD4S014S dual buck converter, Texas Instruments TPS51020 dual buck converter, and Fairchild FAN5026 dual-output PWM controller were commercially available and would have been suitable to implement for use in Harris in view of the FBDIMM Standards. Pet. 37–40.

Patent Owner does not specifically respond to Petitioner's contentions as to claims 2, 3 and 15. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Harris in combination with the FBDIMM Standards teaches the limitations of claims 2, 3, and 15. Based on the current record, Petitioner has established a reasonable likelihood to prevail in showing unpatentability of claims 2, 3, and 15.

6. Determination for Challenge Ground 1

Petitioner has shown a reasonable likelihood to prevail in showing unpatentability of claims 1–3 and 15 as obvious over the combination of Harris and the FBDIMM Standards for the reasons explained.

E. Ground 2: Obviousness Over Harris, the FBDIMM Standards, and Amidi

Petitioner contends claims 1–30 of the '054 patent would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi. Pet. 41–70. For the reasons that follow, we are persuaded that the evidence, including Dr. Wolfe's testimony, sufficiently supports Petitioner's arguments and, therefore, establishes a reasonable likelihood of prevailing with respect to this ground at this stage of the proceeding.

1. Amidi (Ex. 1024)

Amidi was filed on October 25, 2006, issued on May 25, 2010, and is titled "Clock and Power Fault Detection for Memory Modules." Ex. 1024, codes (22), (45), (54). Petitioner contends Amidi is prior art under § 102(e). Pet. 11.

Amidi's Figure 5 is reproduced below.

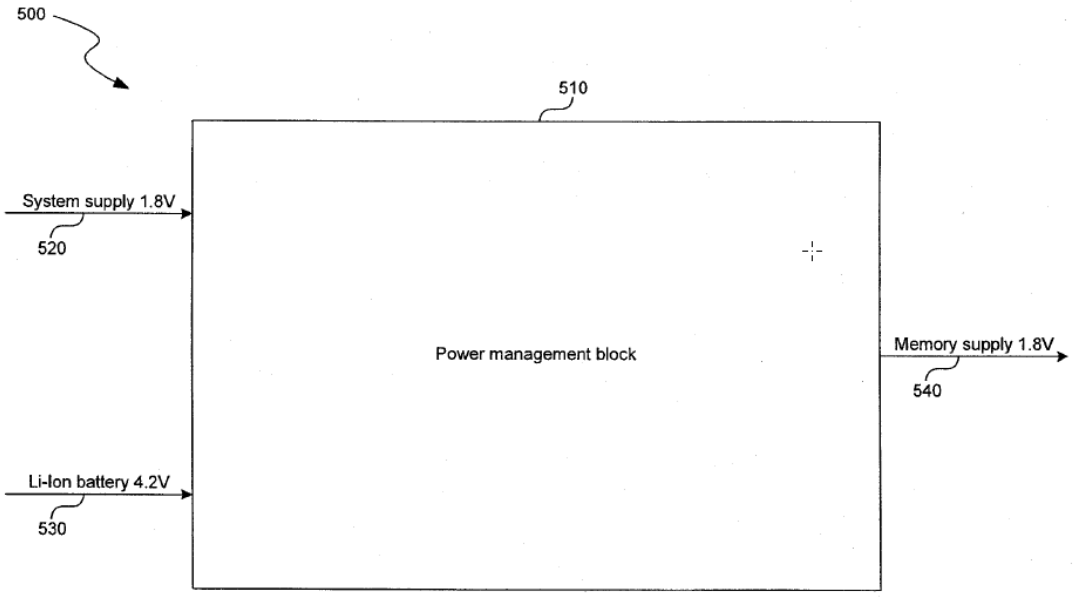


FIG. 5

Amidi's Figure 5 above illustrates a power management block 510 that receives an incoming system supply 520, and incoming battery supply 530, and generates an outgoing memory power supply 540 which is stabilized in the face of disruptions to the system supply 520 using the battery supply 530. Ex. 1024, 4:14–22, 8:23–36, Fig. 5, Fig. 14; Ex. 1003 ¶¶ 131–132.

2. Motivation to Combine

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Harris and the FBDIMM Standards with Amidi with a reasonable expectation of success. Pet. 41. Specifically, Petitioner contends that Harris recognizes concerns with power reliability and proposes the use of a redundant power source. *Id.* (citing Ex. 1023 ¶¶ 12–14, 16, Figs. 1B, 2). Petitioner notes that Amidi teaches a redundant power source (a battery on the memory module) for maintaining data during power disruption. *Id.* at 41–42 (citing Ex. 1024, code (57), 1:28–35, 2:6–26, 4:14–60, Figs. 5–6; Ex. 1003 ¶¶ 171–177). Petitioner further notes that

Amidi's power management block could be modified easily to work with Harris's FBDIMM memory module by changing the system supply 520 and memory supply 540 to 12V as taught by Harris. *Id.* at 42 (citing Ex. 1024, Fig. 5; Ex. 1023 ¶ 12; Ex. 1003 ¶¶ 173–174). Petitioner contends that to a person of ordinary skill in the art it would have been obvious to use the 12V external supply stepped-down with a buck converter to a 5V supply for charging Amidi's battery, and that Amidi's battery voltage would be stepped-up with a boost converter to the 12V level used by Harris's memory module. *Id.* at 42–43 (citing Ex. 1024, Fig. 6 (620); Ex. 1003 ¶¶ 173–174). Petitioner contends that Amidi discloses that its power management block uses "buck" converters to step-down voltages as needed, and "boost" converters to step-up voltages as needed, as had long been taught in textbooks. *Id.* at 43 (citing Ex. 1024, 4:27–32, 4:38–40, Figs. 5, 6; Ex. 1058, 3; Ex. 1032, 161). Petitioner further contends that Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module and the FBDIMM standards, such that a person of ordinary skill in the art would have been motivated to combine their teachings. *Id.* at 43–45.

Petitioner contends that the combination of Harris, the FBDIMM Standards, and Amidi would result in the following configuration and voltage mappings:

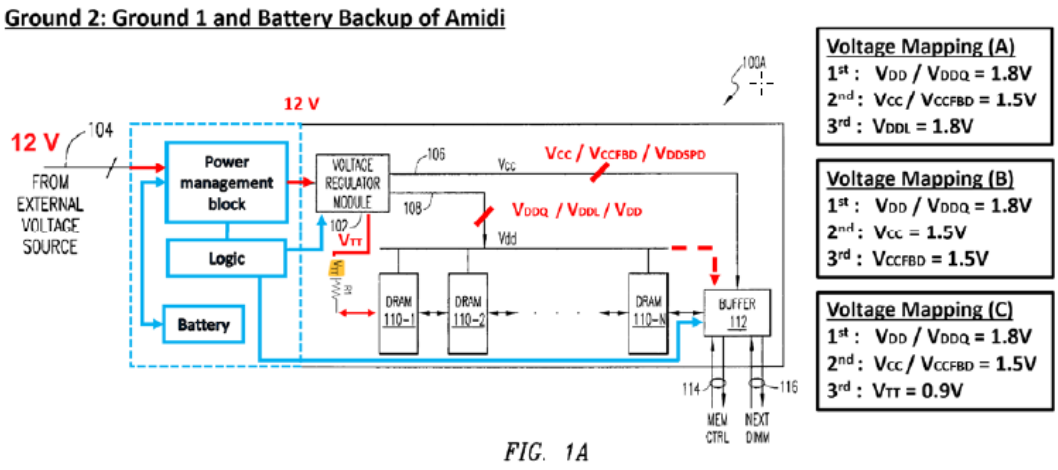


FIG. 1A

Pet. 45. Above, Petitioner has annotated Harris's Figure 1A to show features added from the teachings of the FBDIMM Standards (red) and features added from the teachings of Amidi (blue).

Patent Owner argues that Harris provides alternate voltage sources to power a memory module in the event of a power interruption, so Harris already provides a solution for the alleged problem that Amidi addresses. Prelim. Resp. 35–39. Harris does not appear to describe, however, switching to an alternate voltage source in response to power loss, nor does it explicitly mention a battery as an alternate voltage source, whereas Amidi does. Ex. 1024, code (57). Thus, Patent Owner's argument does not undermine Petitioner's motivation to combine the references.

Patent Owner also argues that "Petitioner has entirely ignored the issue of whether the essential parts of Amidi it seeks to apply to the combination would even fit onto Harris's circuit board, particularly where Petitioner has already proposed to add additional converters." Prelim. Resp. 38–39. Patent Owner's declarant, Dr. Sunil Khatri states that space on the board to fit all of the components that Petitioner proposes would have been a concern. Ex. 2001 ¶¶ 78, n.3, 79. As explained above however, Petitioner

argues that one of ordinary skill would have had reasonable expectation of success in making the combination and supports its argument with credible testimony from Dr. Wolfe who explains how one of ordinary skill would have been able to incorporate Amidi's functionality in the FBDIMM memory module of Harris and that such modification would have been well within the level of skill at the time. Ex. 1003 ¶¶ 171–177.

Accordingly, we determine Petitioner has adequately shown that one of ordinary skill in the art would have been motivated to combine Harris, the FBDIMM Standards, and Amidi with a reasonable expectation of success.

3. Claims 1–3 and 15

We agree with Petitioner that the addition of Amidi does not negate Petitioner's showing with respect to the previous ground. Pet. 45–46 (citing Ex. 1003 ¶¶ 216–301, 431–448). Accordingly, Petitioner has shown a reasonable likelihood to prevail in demonstrating claims 1–3 and 15 unpatentable as obvious over the combination of Harris, the FBDIMM Standards, and Amidi for the reasons stated in the previous ground.

4. Claim 4

Claim 4 depends from claim 1 and recites that the memory module further comprises:

> a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.

Ex. 1001, 38:54–64.

Petitioner points to Amidi's power supervisory module/block 480/665/800 as claim 4's "voltage monitor circuit" coupled to Harris's edge connections for power. Pet. 46. According to Petitioner, Amidi's power supervisory module/block monitors the external system power supply 605/825 in Amidi. *Id.* Petitioner contends that Amidi's power supervisory module/block generates a "trigger signal" corresponding to Amidi's signal 670/858/868. *Id.* Petitioner contends the "predetermined threshold voltage" corresponds to Amidi's reference voltage 675/820 set to 5% or 10% below the nominal voltage of 12V. *Id.* at 46–49 (citing Ex. 1023 ¶¶ 12, 13; Ex. 1003 ¶¶ 303–314; Ex. 1024, 4:8–11, 4:44–52, 5:25–43, 5:31–62, 8:30–62, 8:23–29, 9:8–12, Figs. 4–6, 14, 15). Petitioner further states that the trigger signal causes the memory module to transition from normal operations using an external voltage in the normal range ("the first operable state") to self-refresh operations using a backup battery when the external voltage is outside the normal range ("the second operable state"). *Id.* at 49–50 (citing Ex. 1024, 4:44–52, 8:30–62, 9:8–22, Figs. 6-8, 14, 15; Ex. 1003 ¶¶ 315–321).

Patent Owner does not present any argument specific to claim 4 at this time. *See* Prelim. Resp.

Petitioner has shown sufficiently for institution that claim 4 is obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

5. Claim 5

Claim 5 depends from claim 4 and recites

> a controller coupled to the voltage monitor circuit;
> wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

Ex. 1001, 38:65–39:3.

Petitioner contends that the logic for controlling the S3 sleep mode (Pet. 43–44) corresponds to the claimed "controller" that is coupled to the voltage monitor circuit. Pet. 50–51. Petitioner contends that S3 configuration information is stored in non-volatile memory before entering the S3 sleep mode in response to the trigger signal, satisfying the "wherein" clause of claim 4. *Id.* at 51 (citing Ex. 1003 ¶¶ 322–340).

Patent Owner does not provide any argument specific to claim 5. *See* Prelim. Resp.

Petitioner shows sufficiently that claim 5 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

6. Claims 6, 7, 9–12, and 17

Claims 6, 7, 9–12, and 17 recite, or depend from a claim that recites, that the voltage monitor circuit generates the trigger signal in response to the input voltage being above a predetermined threshold voltage. Ex. 1001, 39:4–20, 39:30–49, 40:21–25. Patent Owner contends that the Petition provides no analysis to explain why one would have configured a memory module to perform a write operation in response to an overvoltage condition. Prelim. Resp. 14–15. Of these claims, only claim 7 requires a write operation to be performed in response to the trigger signal. And Amidi seeks to prevent data loss by storing data in response to detection of an undervoltage situation. On this record, Petitioner's showing for these claims is sufficient for institution. We invite further development of the record at trial before addressing patentability of these claims in a final written decision.

7. Claim 8

Claim 8 depends from claim 1 and recites

> a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections, wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller.

Ex. 1001, 39:21–29.

Petitioner contends that the "controller" corresponds to logic for controlling the S3 sleep mode described in the FBDIMM Standards. Pet. 55 (citing Pet. 43–44). Petitioner contends the controller is coupled to the PCB and includes a "voltage monitor circuit" corresponding to Amidi's power supervisory module/block 480/665/800. *Id.* Petitioner contends Amidi's power supervisory module/block monitors the external system power supply 605/835 ("input voltage") received from Harris's edge connections for power ("a second set of edge connections of the plurality of edge connections"). Pet. 55–56 (citing Pet. 20–25; Ex. 1023, Fig. 1A; Ex. 1024, Fig. 4; Ex. 1027, Ex. 1003 ¶¶ 373–379). Petitioner contends when the external system power supply voltage is too low, Amidi's power supervisory module/block generates signal 670/858/868 ("a signal to one or more portions of the controller") to indicate a power disruption to switch to battery backup and initiate the S3 sleep mode to preserve data in the SDRAMs while conserving power (the "wherein" clause in claim 4). Pet. 56–57 (citing Pet. 46–54; Ex. 1003 ¶¶ 380–285).

Patent Owner does not present any arguments specific to claim 8.

We determine Petitioner shows sufficiently for institution that claim 8 of the '054 patent would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

8. Claim 13

Petitioner contends that claim 13 recites a limitation substantially similar to one addressed with respect to claim 4. Pet. 58 (citing Ex. 1003 ¶¶ 419–423). Patent Owner does not provide specific argument for claim 13. We determine that Petitioner has shown sufficiently that claim 13 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

9. Claim 14

Claim 14 recites

> wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.

Ex. 1001, 39:55–58.

Petitioner contends that a power disruption detected by Amidi's voltage supervisory block 800 causes the system to switch to battery backup. Pet. 61 (citing Pet. 55–57). Petitioner contends that Amidi's voltage supervisory block 800 detects a request by the host system to return control to the host. *Id.* at 61–62 (citing Ex. 1003 ¶¶ 424–430). Petitioner asserts that Amidi "discloses that, if the power is restored after a failure, the voltage supervisory block detects whether the host has cleared the backup-mode bit ('*detecting a request by the host system*') and subsequently, if so, returns control of the module to the host, including handling of the power signal." *Id.* at 62 (citing Ex. 1003 ¶¶ 311, 429; Ex. 1024, 5:31–62, 8:30–62, Fig. 14

9:11–39, Figs. 8, 14 (1460–1490), 15 (steps 1530, 1540, 1570, 1580; Ex. 1003 ¶ 312).

Patent Owner does not separately argue claim 14.

Petitioner shows sufficiently for institution that claim 14 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

10. Claim 16

Petitioner contends that claim 16 is disclosed by the combination of Harris, the FBDIMM Standards, and Amidi for the reasons previously stated for claims 1, 8, and 9, noting that Amidi's voltage supervisory block (e.g., 665) ("the voltage monitor circuit") is "configured to detect an amplitude change in the input voltage" when the external system supply changes by crossing the reference voltage. Pet. 58 n.4 (emphasis omitted).

Patent Owner presents no separate arguments for claim 16 apart from those previously discussed.

Petitioner has shown sufficiently for institution that claim 16 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

11. Claims 18–22 and 26–28

Claim 18 depends from claim 16 and recites

> wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

Ex. 1001, 40:26–32.

Petitioner contends that this limitation is taught by the combination of Harris, the FBDIMM Standards, and Amidi. Pet. 63–65. Petitioner contends that "pre-regulated voltage" means either that the voltage is within the 12V +/- 15% limits described in Harris, or must be pre-regulated on the memory board itself. Pet. 63; Ex. 1023 ¶ 13. For purposes of this Decision, we interpret "pre-regulated voltage" to mean that the voltage is regulated before conversion to a stepped up or down level. *See* Ex. 1001, code (57), 28:53–58, Fig. 16 (1110, 1112). Petitioner contends that Harris discloses external voltage sources that are regulated. Pet. 63 (citing Ex. 1023 ¶¶ 13–14); *see* Ex. 1023 ¶ 14 ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either *regulated* or unregulated, and even including variable voltages." (emphasis added)). Harris's disclosure of regulated voltage sources appears to teach a "pre-regulated voltage," as we understand that term. Petitioner also offers an alternative argument based on Amidi, but we need not address it at this point because Petitioner's first argument is sufficiently persuasive. Pet. 63–64. We welcome any further development of the record on this issue, including the proper interpretation of "pre-regulated voltage."

12. Claim 23

Claim 23 depends from claim 16 and recites

> wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

Ex. 1001, 40:65–41:4.

Petitioner contends that claim 23 is substantially similar to limitations included in claims 4 to 6. We agree that Petitioner's showing for claims 4 and 5 is sufficient for claim 23 because determining an undervoltage condition per claim 4 is detecting a voltage amplitude change per claim 23.

Patent Owner does not submit any argument specific to claim 23. *See* Prelim. Resp.

Petitioner shows sufficiently that claim 23 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

13. Claim 24

Petitioner contends that the limitations of claim 24 were all addressed with respect to claims 1, 16, and 23. Pet. 69–70.

Patent Owner's arguments with respect to claim 24 were previously addressed. *See* Sect. III.E.2, *supra*.

Petitioner has shown sufficiently for institution that claim 24 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

14. Claim 25

Petitioner contends that the limitations of claim 25 were addressed with respect to claims 4 and 16. Pet. 58, 70.

Patent Owner provides no argument specific to claim 25. *See* Prelim. Resp.

Petitioner has shown sufficiently for institution that claim 25 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

15. Claim 29

Claim 29 depends from claim 24 and recites that the voltage monitor circuit is configured to detect whether the input voltage is above or below respective thresholds. Ex. 1001, 42:19–23. Petitioner contends that the limitations of claim 29 were addressed with respect to claims 4, 6, and 17. Pet. 58, 70.

Patent Owner provides no argument specific to claim 29. *See* Prelim. Resp.

Petitioner's showing with respect to the undervoltage condition in claim 4 is sufficient to institute for claim 29.

16. Claim 30

Claim 30 depends from claim 29 and recites that the predetermined threshold voltages are above and below a "specified operating voltage." Ex. 1001, 42:24–27. Petitioner contends that the "specified operating voltage" corresponds to Harris's 12V nominal external voltage. Pet. 57, n.2 (citing Pet. 41–45; Ex. 1023 ¶¶ 12, 13).

Patent Owner does not present any arguments specific to claim 30. *See* Prelim. Resp.

Petitioner has shown sufficiently that claim 30 would have been obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

17. Determination for Challenge Ground 2

Petitioner has demonstrated that a person of ordinary skill in the art would have had reason to combine Harris, the FBDIMM Standards, and Amidi with a reasonable expectation of success. Petitioner has also demonstrated that all of the limitations of at least one claim in this challenge

ground are taught by the combination. Accordingly, under this ground, Petitioner has demonstrated a reasonable likelihood to prevail in showing unpatentability of at least one claim of the '054 patent as obvious over the combination of Harris, the FBDIMM Standards, and Amidi.

F. Ground 3: Obviousness over Harris, the FBDIMM Standards, Amidi, and Hajeck

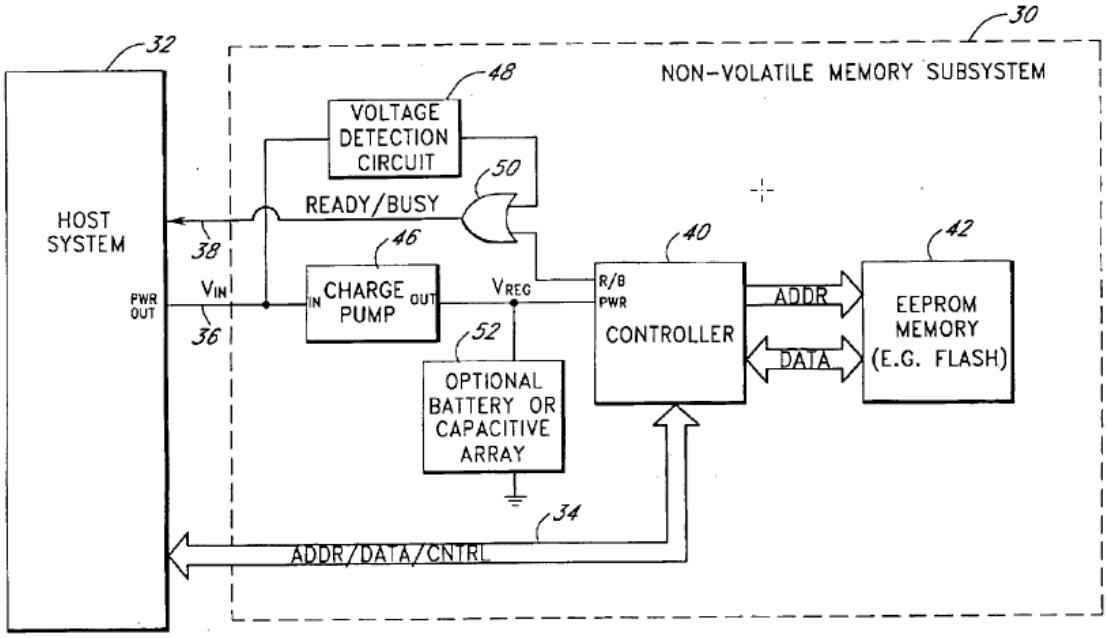
Petitioner contends claims 1–30 would have been obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck. Pet. 70–72.

1. Hajeck (Ex. 1038)

Hajeck is titled "Storage Subsystem with Embedded Circuit for Protecting Against Anomalies in Power Signal from Host." Ex. 1001, code (54). Hajeck issued as U.S. Patent No. 6,856,556 B1 on February 15, 2005. Petitioner contends Hajeck is prior art under § 102(b). Pet. 12.

Hajeck seeks to protect storage subsystems from damage and data loss caused by irregularities in a power signal provided by a host. Ex. 1038, 1:10–13. Specifically, Hajeck seeks to prevent data loss due to loss of power from a host system, and to prevent power surges or spikes from damaging circuitry of the storage subsystem. *Id.* at 1:15–31.

Hajeck's Figure 1 is reproduced below.



In Hajeck's Figure 1, non-volatile memory subsystem 30 receives power from host system 32 at charge pump 46 which supplies regulated voltage to controller 40. *Id.* at 2:64–67. In the event of a power surge or spike, charge pump 46 protects controller 40 from damage. *Id.* at 3:12–16. In the event of a voltage drop, charge pump 46 with battery and capacitive array 52 provides sustained voltage to controller 40. *Id.* at 2:60–63, 3:10–13. Voltage detection circuit 48 detects anomalies in the input voltage and generates a "busy" signal provided to the host system 32 to block the host system from performing write operations to the storage subsystem. *Id.* at 1:64–67, 3:30–33.

2. Motivation to Combine

Petitioner contends that one of ordinary skill in the art would have been motivated to combine Hajeck with Harris, the FBDIMM Standards, and Amidi because one would have appreciated the desirability of switching to backup power in both undervoltage and overvoltage conditions.

Pet. 71–72. Hajeck teaches to use a battery backup in response to power loss from the host system to complete outstanding operations and to use the charge pump to protect the controller from surges or spikes in the power supply. *See. e.g.*, Ex. 1038, code (57). Hajeck also teaches a voltage detection circuit generate a "busy" signal in response to undervoltage or overvoltage conditions. *Id.* at 3:30–43. Accordingly, Petitioner's motivation to combine is sufficient for purposes of institution. We invite further development of the record on the parties' views of on the combination of Hajeck with Harris, the FBDIMM Standards, and Amidi.

3. Determination for Ground 3

Petitioner has shown a reasonable likelihood to prevail in demonstrating that claims 1–30 of the '054 patent would have been obvious over the combination of Harris, the FBDIMM Standards, Amidi, and Hajeck.

G. Ground 4: Obviousness over Spiers and Amidi

Petitioner contends that claims 1–30 are obvious over the combination of Spiers and Amidi. Pet. 72–125.

1. Spiers (Ex. 1025)

Spiers is titled "Non-Volatile Memory Backup for Network Storage System." Ex. 1025, code (54). Spiers was filed on October 12, 2004, and published on April 13, 2006 as U.S. Patent Pub. No. 2006/0080515 A1. *Id.* at codes (10), (43). Petitioner contends that Spiers is prior art under § 102(b). Pet. 13.

Spiers's Figure 4 is reproduced below.

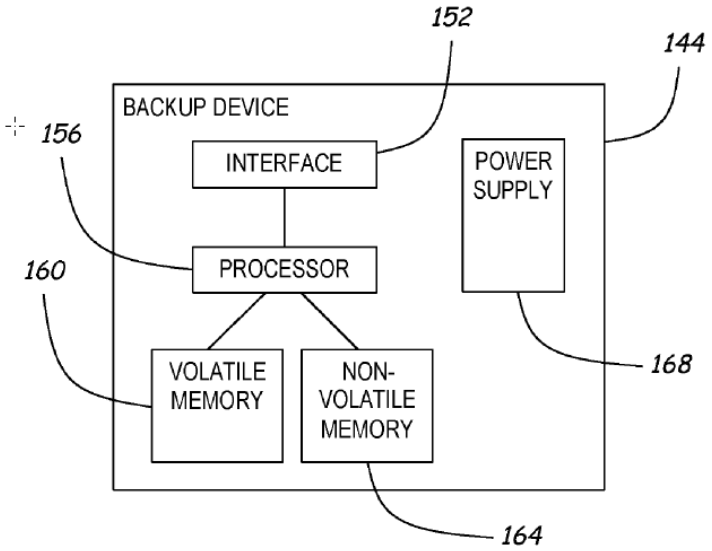


FIG.4

Spiers's Figure 4 above shows backup device 144. Ex. 1025 ¶ 36. Backup device 144 comprises an interface 152, backup device processor 156, volatile memory 160, non-volatile memory 164, and power supply 168. *Id.* Interface 152 communicates with storage controller 132 (not shown). *Id.* Interface 152 connects to processor 156 which controls operations within backup device 144. *Id.* Processor 156 connects to volatile memory 160 and non-volatile memory 164. *Id.* Volatile memory 160 may be an SDRAM used to store data from storage controller 132 during typical write operations. *Id.* Non-volatile memory 164 may be flash memory and is used in the event of a power failure detection. *Id.* Upon detecting a power failure, processor 156 switches backup device 144 to power supply 168 (capacitors or batteries) and moves data in volatile memory 160 to non-volatile memory 164. *Id.*

2. Motivation to Combine

Petitioner contends that one of ordinary skill in the art would have been motivated to combine Spiers and Amidi. Pet. 73–77. Petitioner

contends one would have used Amidi to learn implementation details, such as specific type of SDRAM devices and voltage regulators, useful for Spiers. *Id.* at 73 (citing Ex. 1003 ¶¶ 197–201). Petitioner contends while Spiers teaches SDRAM devices, Amidi specifically discloses DDR SDRAM devices. *Id.* at 74 (citing Ex. 1024, claims 4–5). Petitioner contends a person of ordinary skill in the art would have been motivated to implement Spiers with commercially available DDR2 or DDR3 SDRAMs powered according to relevant JEDEC standards with a reasonable expectation of success when using such well-known, standardized technology. *Id.* (citing Ex. 1003 ¶¶ 199–201).

Patent Owner argues that Spiers only mentions two voltage regulators, and that Petitioner provides no reason why a person of ordinary skill in the art would have used DDR2 or DDR3 devices, which require more than two regulated voltages, instead of the SDR SDRAM devices specified by Spiers. Prelim. Resp. 39–40. Petitioner contends that Amidi provides a reason to use DDR2 or DDR3 SDRAMs powered according to relevant JEDEC standards. Pet. 74 (citing Ex. 1003 ¶¶ 199–201). Patent Owner contends that Spiers's writes to SDRAM occur with every system write, and that Petitioner makes no showing that DDR2/DDR3 devices would have been used for such a high write-to-read ratio application. Prelim. Resp. 40 (Ex. 2001 ¶ 90; Ex. 1025 ¶¶ 34, 36, 40, 41, Figs. 11, 12).

Patent Owner's evidence does not establish that DDR2 or DDR3 devices would not work in Petitioner's combination, only that they would be sub-optimal in that application. On the current record, we cannot determine that such a solution would be sufficiently sub-optimal that one of ordinary skill in the art not have pursued it, but instead would have looked to some

other unidentified solution. *See also Novartis Pharms. Corp. v. West-Ward Pharms. Int'l Ltd.*, 923 F.3d 1051, 1059 (Fed. Cir. 2019) (noting that an obviousness showing "does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention." (quoting *In re Fulton*, 391 F.3d 1195, 1200 (Fed. Cir. 2004))).

Patent Owner also argues that SDRAM devices could operate at or above the data rates of a PCI interface used by Spiers, so replacing Spiers's SDRAM devices with faster DDR2 or DDR3 would not bring about a gain in data rate or justify the added expense of additional voltage regulators to accommodate DDR2/DDR3 devices. Prelim. Resp. 41 (citing Ex. 2001 ¶¶ 91–95).

Patent Owner's argument assumes that Spiers is limited to a PCI interface, but a PCI backup device is described as one embodiment in Spiers. Ex. 1025 ¶ 19. Spiers also discloses an "interface 152" in more general terms, which does not appear limited to a PCI interface. *Id.* ¶ 36. Patent Owner has not shown that the interfaces that one of ordinary skill in the art would have considered to use in light of Spiers would not have been able to accommodate faster DDR2/DDR3 devices. Accordingly, this argument is not persuasive on the record as thus far developed.

Petitioner has shown sufficiently that one of ordinary skill in the art would have combined Spiers and Amidi.

3. Claim 1

a) Limitation 1.a: "A memory module comprising:"

Petitioner contends that Spiers discloses this limitation. Pet. 77–78. Petitioner contends that Spiers's backup device 144 corresponds to the

claimed "memory module." *Id.* at 77. Spiers's backup module 144 has both volatile memory (SDRAMs 190) and non-volatile memory (NAND flash 194). *Id.* at 77–78.

Patent Owner does not specifically respond to these arguments. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Spiers teaches this limitation for purposes of institution.

> *b) Limitation 1.b: "a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system"*

Petitioner contends that Spiers discloses this limitation. Pet. 79–81. Petitioner asserts that Spiers's PCI card corresponds to "a printed circuit board (PCB)." *Id.* at 79. Petitioner contends that Spiers's PCI card has an interface configured to fit into the slot connector of a host system, and including a plurality of edge connections. *Id.* (citing Ex. 1025, Fig. 5). Petitioner contends these edge connections are configured to couple power, data, address and control signals between the memory module and host system. *Id.* (citing Ex. 1025 ¶¶ 37, 39, 54; Ex. 1031, 1, 7, 21–25, 146–150).

Patent Owner submits no argument specific to this limitation. *See* Prelim. Resp.

Based on our review and consideration of the current record, we determine that Petitioner has adequately shown that Spiers teaches this limitation for purposes of institution.

> *c) Limitation 1.c: "a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages"*

Petitioner contends that Spiers's power supply 168 discloses a voltage conversion circuit coupled to the PCB and configured to provide three regulated voltages when backup device 144 is implemented with DDR2 or DDR3 DRAMs according to Petitioner's voltage mappings. Pet. 81–84. Petitioner relies on Amidi to disclose use of buck converters to supply the regulated voltages specified by the JEDEC standards for DDR2 or DDR3 DRAMs. *Id.* at 85–86. In addition, Petitioner identifies commercially available buck converters for use in implementing the proposed combination. *Id.* at 87–88.

Patent Owner contends that Petitioner has not shown why one would have required three buck converters for use in Spiers. Prelim. Resp. 52–70. As mentioned, Petitioner contends that to supply the regulated voltages specified in the JEDEC standards for DDR2 or DDR3 DRAMs or FBDIMMs, at least three buck converters would be required. Pet. 81–86.

Patent Owner contends that Petitioner did not provide any evidence why one would need to use V_{TT} in the DDR2 or DDR3 standards. Prelim. Resp. 53–56. However, even if Patent Owner is correct, Petitioner did not rely solely on V_{TT} as the third regulated voltage. *See* Pet. 82.

Patent Owner argues there is no evidence that one would have generated V_{TT} using a buck converter. Prelim. Resp. 56–59. Petitioner explained that the reason for using a buck converter for regulated voltages comes from Amidi. *See* Pet. 86 (citing Ex. 1024, Fig. 6 (640), 4:38–41).

Patent Owner further argues that Petitioner provided no reason for equipping Spiers with multiple 1.8V regulators. Prelim. Resp. 59–60. Assuming Patent Owner is correct, Petitioner also provided Voltage Mapping A which does not require the same voltage to be used for the regulated voltages. *See* Pet. 82. Petitioner also explained that the JEDEC standards provide for separate pins with the same voltage levels, and that certain voltages should be isolated and separately controlled to provide independence, stability, and flexibility for power management. Pet. 30.

Patent Owner further argues there are other ways to generate regulated voltages than providing a buck converter for each voltage level, and Petitioner did not show why one would not have pursued these other options. Prelim. Resp. 60–70. Petitioner did explain, however, that using a buck converter for each regulated voltage would "achieve high efficiency, reliability, and flexible power conversion." Pet. 85 (citing Pet. 29–30).

Petitioner has shown sufficiently for institution that the combination of Spiers and Amidi teaches this claim limitation.

> *d) Limitation 1.d.1: "a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages"*

Petitioner contends that Spiers's DRAM, FPGA/processor, termination resistors, and non-volatile memory are components coupled to the PCI card, which are each coupled to at least one of three regulated voltages. Pet. 89.

Patent Owner provides no argument specific to this limitation. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

> *e) Limitation 1.d.2: "the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and"*

Petitioner asserts that Spiers discloses SDRAMs 190 that may be implemented as DDR2 or DDR3 devices. Pet. 90.

Patent Owner provides no argument specific to this limitation. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

> *f) Limitation 1.d.3: "a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections"*

Petitioner contends that the "first circuit" corresponds to Spiers FPGA processor 198 coupled to the SDRAM devices 190, 218 and to the PCI interface 172 for data, address and control signals. Pet. 90–91.

Patent Owner does not specifically respond to Petitioner's contention. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

> *g) Limitation 1.d.4: "wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and"*

Petitioner contends that Spiers's FPGA processor 198 couples to voltage V_{DD}/V_{DDQ} (1.5V) and V_{CCFPGA} (1.8V). Pet. 91–92.

Patent Owner does not specifically address Petitioner's contention for this limitation. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

h) Limitation 1.d.5: "wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages"

Petitioner contends that Spiers's SDRAM devices are coupled to the regulated voltage V_{DD}/V_{DDQ} (1.5V or 1.8V). Pet. 92.

Patent Owner does not specifically respond to Petitioner's contention. *See* Prelim. Resp.

Petitioner has adequately shown that the combination of Spiers and Amidi teaches this limitation for purposes of institution.

i) Determination for Claim 1

Petitioner shows sufficiently that one of ordinary skill in the art would have had reason to combine Spiers and Amidi with a reasonable expectation of success in arriving at claim 1. Furthermore, Petitioner has shown sufficiently that the combination of Spiers and Amidi teaches each limitation of claim 1. Accordingly, Petitioner has established a reasonable likelihood to prevail in showing that claim 1 is unpatentable as obvious over the combination of Spiers and Amidi.

4. Claims 2—30

We have reviewed Petitioner's contentions for each of claims 2–30, and find them sufficient to disclose the limitations recited in at least claims 2, 5, 8, 13, 14, 16, 23, 25, 29 and 30. Pet. 92–125.

Other than the arguments previously addressed under claim 1, Patent Owner does not present further any argument specific to these claims. *See* Prelim. Resp.

Petitioner has shown sufficiently that the combination of Spiers and Amidi discloses at least one of these claims.

Accordingly, Petitioner has established a reasonable likelihood to prevail in showing at least one of these claims is unpatentable as obvious over the combination of Spiers and Amidi under this ground.

H. Ground 5: Obviousness over Spiers, Amidi, and Hajeck

Petitioner contends that a person of ordinary skill in the art would have combined Hajeck with Spiers and Amidi because Hajeck teaches the importance of detecting both undervoltage and overvoltage conditions to avoid data loss. Pet. 26. Hajeck teaches generating a busy signal for a host in response to undervoltage or overvoltage conditions. Ex. 1038, 3:44–61. Hajeck also teaches that its charge pump protects its controller from being damaged by spikes and surges in a power signal provided by a host. *Id.* at 3:13–16. Petitioner has shown sufficiently that one of ordinary skill in the art would have been motivated to combine Hajeck with Spiers and Amidi to detect undervoltage and overvoltage conditions. We invite elaboration of the parties views' concerning the combination of Spiers, Amidi and Hajeck at trial.

On this record, Petitioner's showing is sufficient to present a reasonable likelihood that claims 1–30 are unpatentable as obvious over the combination of Spiers, Amidi, and Hajeck. Pet. 125–127. And this ground subsumes the previous one, and there is no persuasive evidence that Hajeck negates Spiers and Amidi. Accordingly, Petitioner has presented a reasonable likelihood to prevail in showing at least one of claims 1–30 is unpatentable as obvious over the combination of Spiers, Amidi, and Hajeck under this ground.

IV. CONCLUSION

After considering the evidence and arguments presented in the Petition and Preliminary Response, we determine that Petitioner has established a reasonable likelihood of prevailing on its assertion that at least one claim of the '054 patent is unpatentable. Accordingly, we institute an *inter partes* review on all the challenged claims and all of the grounds presented in the Petition. At this stage of the proceeding, we have not made a final determination as to the patentability of these challenged claims.

V. ORDER

In consideration of the foregoing, it is hereby

ORDERED that pursuant to 35 U.S.C. § 314, *inter partes* review is instituted as to the challenged claims of the '054 patent with respect to all grounds of unpatentability presented in the Petition; and

FURTHER ORDERED that *inter partes* review is commenced on the entry date of this Order, and pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial.

IPR2022-00999
Patent 11,232,054 B2

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Paper 14
Entered: October 21, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO. LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00711
Patent 10,860,506 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and NABEEL U. KHAN, *Administrative Patent Judges*.

KHAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co. Ltd. [1] ("Petitioner") filed a Petition (Paper 1, "Pet.") requesting an *inter partes* review of claims 1–20 ("the challenged claims") of U.S. Patent No. 10,860,506 B2 ("the '506 patent," Ex. 1001). Netlist, Inc. ("Patent Owner") timely filed a Preliminary Response (Paper 7, "Prelim. Resp.").

An *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on at least one of the challenged claims of the '506 patent, and we institute an *inter partes* review as to the challenged claims of the '506 patent on all the grounds of unpatentability set forth in the Petition.

B. Related Proceedings

The parties identify the following matters as related to this case:

- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, Case No. 1:21-cv-01453 (D. Del.);
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, Case No. 2:21-cv-00463 (E.D. Tex.);
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 1:22-cv-00136 (W.D. Tex.);

[1] Petitioner also identifies Samsung Semiconductor, Inc. as a real party-in-interest. Pet. xxiii.

- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00236 (PTAB);
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00237 (PTAB); and
- U.S. Patent Application No. 17/114,478.

Pet. xxiii; Paper 8, 1.

C. The '506 Patent (Ex. 1001)

The '506 patent, titled "Memory Module with Timing-Controlled Data Buffering," relates to a memory system that controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 2A, reproduced below, illustrates a memory module. *Id.* at 4:65–66.

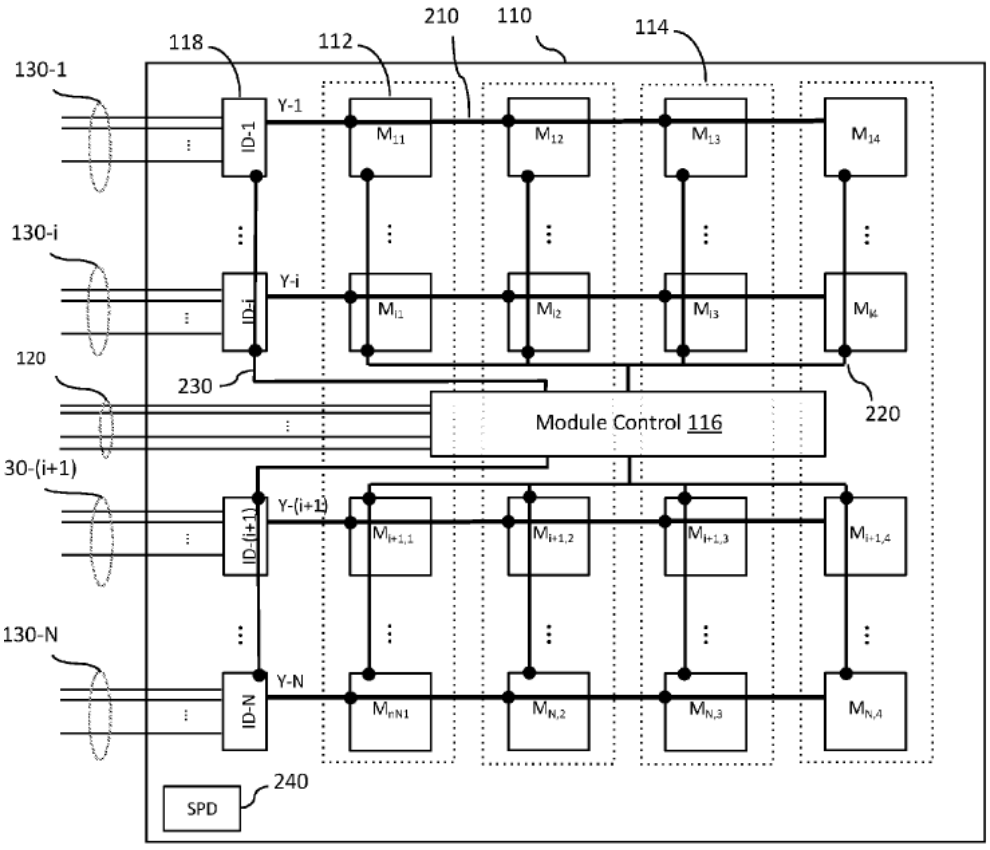

FIG. 2A

As shown in Figure 2A, memory module 110 includes module control device 116 and plurality of memory devices 112. Ex. 1001, 4:65–67, 6:4–8.

Memory module 110 further includes control/address signal lines 120 and data/strobe signal lines 130, which are coupled to a memory controller (MCH) (not shown). *Id.* at 4:20–25. Respective groups of data/strobe signal lines 130 are also coupled to respective isolation devices, or buffers, 118, *e.g.*, group of data/strobe signal lines 130-1 is coupled to isolation device ID-1. *Id.* at 4:30–32; *see id.* at 3:27–29, 6:17–20. Furthermore, each isolation device 118 is associated with, and coupled to, a respective group of memory devices via module data/strobe lines 210. *Id.* at 6:17–20, 6:30–32. For example, as shown along the top of memory module 110, isolation device ID-1 "is associated with [a] first group of memory devices M_{11}, M_{12}, M_{13}, and M_{14}, and is coupled between the group of system data/strobe signal lines 130-1 and the first group of memory devices" via module data/strobe lines 210. *Id.* at 6:20–25.

In operation, memory module 110 "perform[s] memory operations in response to memory commands (*e.g.*, read, write, refresh, precharge, etc.)." Ex. 1001, 3:30–32. Those commands are transmitted over control/address signal lines 120 and data/strobe signal lines 130 from the memory controller. *Id.* at 3:29–34, 4:20–25, 4:65–5:1. For example, "[w]rite data and strobe signals from the controller are received and buffered by the isolation devices 118 before being transmitted to the memory devices 112 by the isolation devices 118." *Id.* at 7:63–66. And, "read data and strobe signals from the memory devices are received and buffered by the isolation devices before being transmitted to the MCH via the system data/strobe signal lines 130." *Id.* at 7:66–8:3.

As can be seen in Figure 2A, and as the '506 patent explains, there are "unbalanced" lengths of control wires to respective memory devices, which cause a "variation of the timing" of signals due to the variation in wire

length. *See* Ex. 1001, 2:20–30; *see also id.* at 8:26–55. To account for timing issues, each isolation device, or data buffer, 118 is "responsible for providing a correct data timing" and "for providing the correct control signal timing." *Id.* at 8:64–9:3. In particular, "isolation devices 118 includes [a] signal alignment mechanism to time the transmission of read data signals based on timing information derived from a prior write operation." *Id.* at 15:23–26. For example, because write signals are received by isolation device 118, isolation device 118 uses that knowledge and determines timing information that is used to "properly time transmission" of a later read operation. *Id.* at 15:42–50.

D. Illustrative Claims

Claims 1 and 14 are the independent claims of the '506 patent. Claim 1, which is representative of the challenged claims, is reproduced below with limitation identifiers in brackets corresponding to claim analysis headings in the Petition. *See* Pet. 20–38.

> 1. [pre] A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus , the memory module comprising:
>
> [a] a module board having edge connections to be coupled to respective signal lines in the memory bus;
>
> [b] a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;
>
> [c1] memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals, [c2] wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read

> data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and
>
> [d] data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and [e] wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:
>
> > [f] delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;
> >
> > [g] sample the first section of the read data using the first delayed read strobe; and
> >
> > [h] transmit the first section of the read data to a first section of the data bus;
>
> [i] wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.

Ex. 1001, 19:16–55.

E. Evidence

The Petition relies on the following references:

Reference	**Exhibit No.**
US 2010/0312956 A1; filed June 3, 2010; published Dec. 9, 2010 ("Hiraishi").	1005
US 8,020,022 B2; filed Sept. 12, 2008; issued Sept. 13, 2011 ("Tokuhiro").	1006
US 2006/0277355 A1; filed June 1, 2005; published Dec. 7, 2006 ("Ellsberry").	1007
US 6,184,701 B1; filed May 27, 1999; issued Feb. 6, 2001 ("Kim").	1008

Reference	Exhibit No.
US 2007/0008791 A1; filed July 7, 2005; published Jan. 11, 2007 ("Butt").	1029

Petitioner also relies on the Declaration of Robert G. Wedig, Ph.D. (Ex. 1003) in support of its arguments. The parties rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–20 are unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)[2]	Hiraishi, Butt
3, 5, 12, 16	103(a)	Hiraishi, Butt, Ellsberry
8–10, 19, 20	103(a)	Hiraishi, Butt, Kim
1, 2, 4, 6, 7, 11, 13–15, 17, 18	103(a)	Hiraishi, Butt, Tokuhiro
3, 5, 12, 16	103(a)	Hiraishi, Butt, Tokuhiro, Ellsberry
8–10, 19, 20	103(a)	Hiraishi, Butt, Tokuhiro, Kim

II. ANALYSIS

A. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent

[2] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. For this proceeding, Petitioner assumes that the '506 patent has an effective priority date before this date (Pet. 2) and applies the pre-AIA version of § 103.

Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Petitioner contends a person of ordinary skill in the art "would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and at least three years of work experience in the field." Pet. 2 (citing Ex. 1003 ¶ 37). Patent Owner asserts it is "applying the level of ordinary skill in the art proposed by Petitioner." Prelim. Resp. 11.

For purposes of this Decision, we adopt Petitioner's proposed level of ordinary skill, except that we find that the phrase "at least" in Petitioner's proposed definition creates a vague, open-ended upper bound for the level of ordinary skill, and we therefore do not adopt that aspect of the proposal. Thus, we determine at this stage of the proceeding, that a person of ordinary skill in the art would have been a person with an advanced degree in electrical or computer engineering and two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and three years of work experience in the field.

C. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2020).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Neither party proposes any constructions for any claim terms. *See* Prelim. Resp; *see also* Pet. 9.[3] We determine no terms need to be construed to resolve the disputes between the parties at this stage of the proceeding.

D. Obviousness over Hiraishi and Butt (Ground 1)

Petitioner argues claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 of the '506 patent would have been obvious over Hiraishi and Butt. Pet. 20–68. Below we provide a brief overview of the prior art references and analyze Petitioner's contentions in light of Patent Owner's arguments.

1. Hiraishi (Ex. 1005)

Hiraishi relates to a memory module having memory chips and data register buffers arranged in a manner that shortens data line lengths. Ex. 1005, code (57). Figure 1, reproduced below, is "a schematic diagram of a configuration of a memory module." *Id.* ¶ 13.

[3] Petitioner indicates that it may assert in the related District Court case that "certain terms in the '506 [p]atent are subject to § 112, ¶ 6, and indefinite for failure to disclose an adequate structure or algorithm," but, for purposes of its Petition, "adopts Patent Owner's current position on claim construction that § 112, ¶ 6 does not apply." Pet. 9–10.

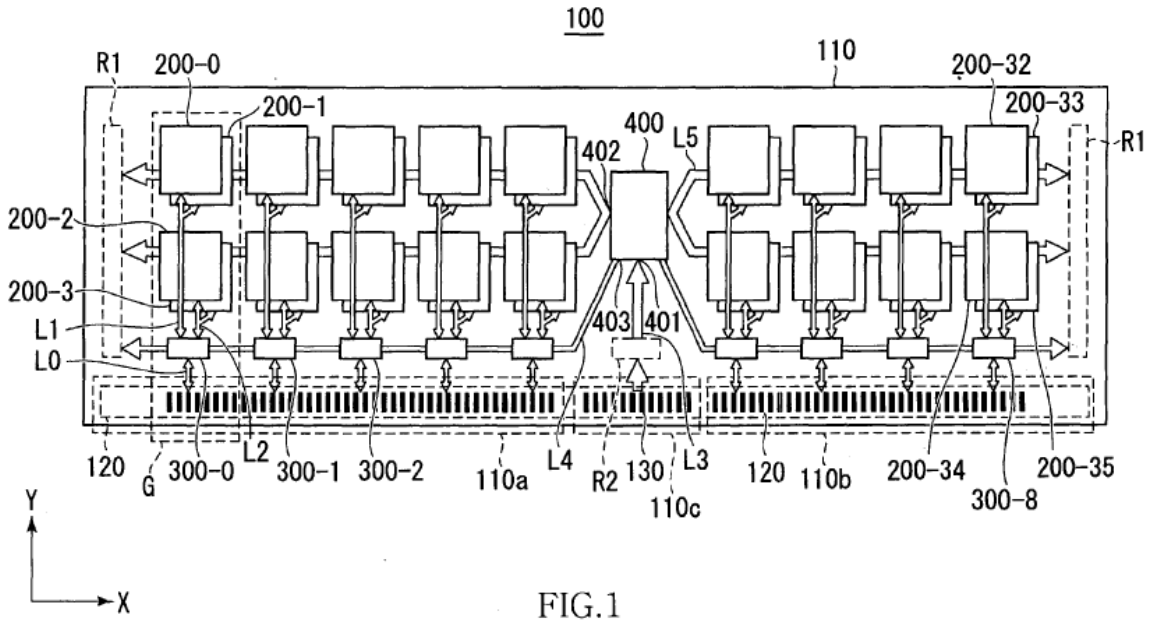

FIG.1

As shown in Figure 1, memory module 100 includes "a plurality of memory chips 200 mounted on [a] module substrate 110." Ex. 1005 ¶ 45. Further, memory module 100 includes nine data register buffers 300-0 to 300-8 and address/control register buffer 400. *Id.* ¶ 46. Still further, memory module 100 includes "data connectors 120[, which] are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and [a] memory controller" electrically connected to the connectors. *Id.* ¶¶ 47–48 (memory controller not shown). As can be seen in Figure 1, and as further detailed in Figure 7, "data register buffer 300 intervenes between the data connectors 120 and the memory chips 200." *Id.* ¶ 103. Figure 7, reproduced below, is a connection diagram of memory module 100. *Id.* ¶ 19.

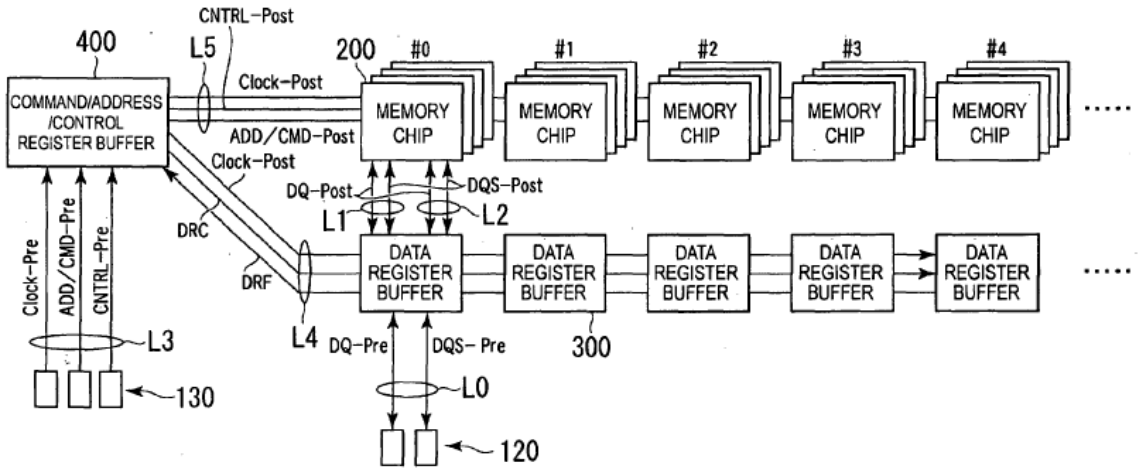

FIG.7

As shown in Figure 7, "data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2." Ex. 1005 ¶ 103. "[A] data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post." *Id.*

Further, "[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post." *Id.* ¶ 104. As such, "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller." *Id.* Hiraishi "adjust[s] a write timing or a read timing in consideration of a propagation time of a signal" via leveling operations. *Id.* ¶ 140. The write leveling and read leveling operations are provided via write leveling and read leveling circuits in the data register buffer, as shown in Figure 5, which

is a block diagram of the configuration of the data register buffer 300 and is reproduced below. *Id.* ¶ 83.

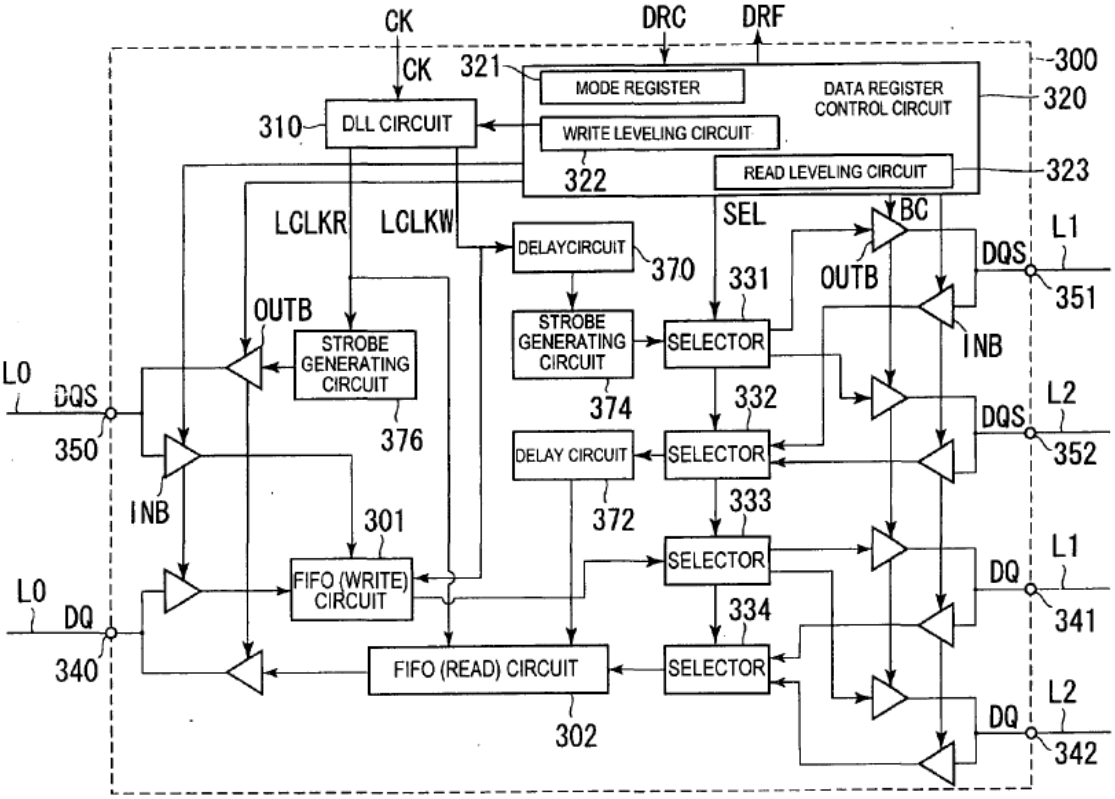

FIG.5

As shown in Figure 5, data register buffer 300 includes write leveling circuit 322 and read leveling circuit 323. Ex. 1005 ¶¶ 90, 145, 147. The write leveling and read leveling operations "adjust a write timing or a read timing in consideration of a propagation time of a signal." *Id.* ¶ 140. For example, in a write operation, "[b]ecause it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side." *Id.* ¶ 143. To compensate for that, "write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS." *Id.* ¶ 145.

An exemplary read leveling operation also adjusts signal timing for a read operation. *See* Ex. 1005 ¶¶ 147–151. For example,

> read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Id. ¶ 151.

2. Butt (Ex. 1029)

Butt relates to DQS strobe centering that is "suitable for a DDR memory application." Ex. 1029 ¶ 2. Figure 2, reproduced below, is a "detailed block diagram of a read data logic and signal paths of a memory interface." *Id.* ¶ 9.

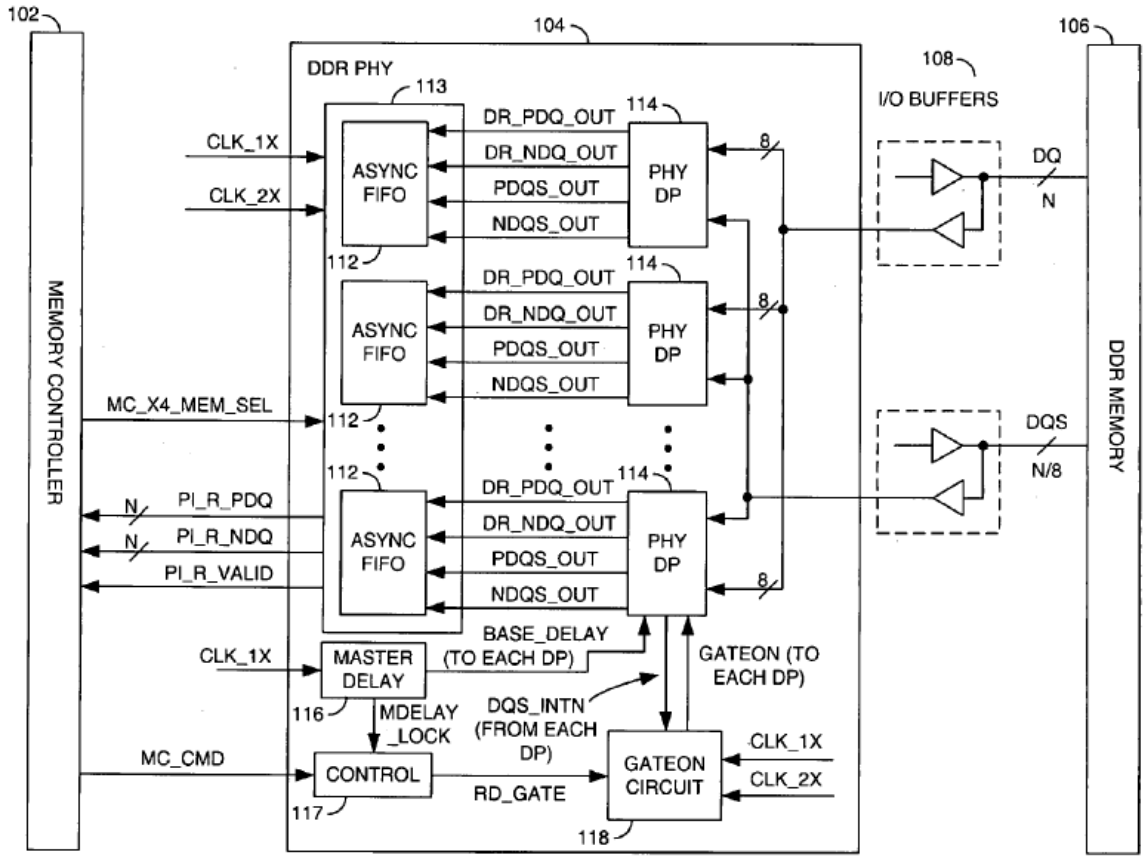

FIG. 2

As shown in Figure 2, a system includes memory controller 102, memory interface 104, and one or more double data rate (DDR) synchronous dynamic random-access memory (SDRAM) devices 106. Ex. 1029, ¶¶ 15, 17. The circuit 104 comprises "a number of asynchronous (ASYNC) first-in first-out (FIFO) buffers 112, FIFO synchronization logic 113, a number of physical read datapaths (DPs) 114, a master delay (MDELAY) logic 116, a control logic 117 and a programmable gating signal generator 118." *Id.* ¶ 17. Each of the physical read datapaths 114 is "configured to receive (i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal or signals DQS associated with the respective portion of the received read data signals and (iii) a gating signal

(e.g., GATEON) from the programmable gating signal generator 118." *Id.* The DPs are "configured via internal settings to delay the read data strobe signals DQS based on one or more control signals (or values) from the MDELAY circuit 116." *Id.* ¶ 18.

3. Analysis of Claim 1

a) Preamble and Undisputed Limitations 1[a]–1[e]

Petitioner provides detailed analysis demonstrating that Hiraishi and Butt teach the preamble and limitations 1[a]–1[e]. Pet. 21–35. Petitioner supports its arguments with citations to Hiraishi and Butt and to the testimony of Dr. Wedig. *Id.* Patent Owner does not separately dispute Petitioner's contentions regarding the preamble and these limitations. At this stage of the proceeding, we are persuaded that Petitioner has demonstrated a reasonable likelihood that Hiraishi and Butt teach the preamble and limitations 1[b]–1[e] for the reasons provided by Petitioner, which we summarize below.

For example, for the preamble Petitioner identifies Hiraishi's memory module 100 as teaching the recited "memory module," memory control hub (MCH 12) as teaching the recited "memory controller," and bus 23 with data lines L0 as teaching the recited "data bus." Pet. 21 (citing Ex. 1005 ¶¶ 65, 69, Figs. 1–3; Ex. 1003 ¶¶ 101–102). Petitioner argues that Hiraishi's memory module 100 connects to MCH 12 by a memory bus 23 and that bus 23 includes a set of control/address signal lines. *Id.* at 22–23 (citing Ex. 1005 ¶¶ 47, 49, 60, 69, 102–103, 107, Figs. 1, 3, 7; Ex. 1003 ¶¶ 102–103).

For limitation 1[a] Petitioner identifies Hiraishi's module substrate 110 as the recited "module board," and command/address/control connectors 130 and data connectors 120 as the recited "edge connections." Pet. 23 (citing Ex. 1005 ¶¶ 45, 47–49, Fig. 1; Ex. 1003 ¶¶ 104–107).

For limitation 1[b] Petitioner identifies Hiraishi's command/address/control register buffer 400 as the recited "module control device on the module board." Pet. 24–25 (citing Ex. 1005 ¶ 59, Fig. 1; Ex. 1003 ¶¶ 108–109). Petitioner argues Hiraishi's register buffer 400 is configurable to receive C/A signals corresponding to a read operation through command/address/control connectors 130 and line L3 and to output C/A signals and control signals such as the DRC and Clock-Post signal on line L5. *Id.* at 25 (citing Ex. 1005 ¶¶ 18–19, 47, 60, 97, 99, Figs. 1, 6, 7; Ex. 1003 ¶ 110).

For limitation 1[c1] Petitioner argues that Hiraishi teaches memory devices, depicted in Figure 5 as 200-0 to 200-35, arranged in four different ranks on module board 110 and coupled to register buffer 400 by data line L5. Pet. 28–29 (citing Ex. 1005 ¶¶ 45, 50–52, 107, Figs. 1, 7; Ex. 1003 ¶¶ 114–116).

For limitation 1[c2] Petitioner argues that Hiraishi's memory devices 200 are situated in ranks and correspond to respective sets of data/strobe signal lines such as line L0 depicted in Figure 7 and are connected to data register buffers. Pet. 30 (citing Ex. 1005 ¶¶ 51–54, 56, 76, 79–80, 103, 120–129, Figs. 1, 4, 7; Ex. 1003 ¶ 119). Petitioner argues that, consistent with the JEDEC standard, read commands include a chip select signal that command all memory devices in the selected rank to perform the command together. *Id.* at 30–31 (citing Ex. 1021 at 319, 413; Ex. 1020, 13, 22, 34 n.1; Ex. 1018, 4.20.4-6, 4.20.4-10–4.20.4-16; Ex. 1003 ¶¶ 120–121).

For limitation 1[d] Petitioner argues that Hiraishi's data register buffers 300 are positioned between the set of memory devices 200 and the connectors 120 connecting to the data line L0 and that the data register buffers 300 are coupled to memory devices 200. Pet. 31 (citing Ex. 1003

¶¶ 122–126). Petitioner argues that data buffer 300 receives module command/address/control line L4 from command/address/control register buffer 400. *Id.* at 31–33 (citing Ex. 1005, Figs. 1, 5, 7; Ex. 1003 ¶¶ 122–126).

For limitation 1[e] Petitioner argues that Hiraishi teaches a first data buffer (data register buffer 300) that is coupled to the first memory device (memory devices 200) and is configurable to perform the operations further recited in limitations 1[f] to 1[i] as further explained below. Pet. 34 (citing Ex. 1005 ¶¶ 45, 55–56, 84, 99, 103, Figs. 1, 7; Ex. 1003 ¶¶ 127–128).

b) Limitations 1[f] and 1[i]

Limitations 1[f] and 1[i] require that in response to one or more of the module control signals, the first data buffer is configurable to: 1[f] "delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;" 1[i] "wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations." Ex. 1001, 19:44–55. Petitioner relies on Hiraishi alone and, in the alternative, on the combination of Hiraishi and Butt as teaching these limitations.

With respect to Hiraishi alone, Petitioner argues that Hiraishi's data register buffers (300) include delay circuit 372 and can delay the first read strobe (DQS signal at input 351) by about 90 degrees to generate a first delayed read strobe to the FIFO (Read) Circuit 302. Pet. 35 (citing Ex. 1005 ¶ 91, Fig. 5; Ex. 1003 ¶¶ 99–100). Petitioner argues that Hiraishi's reference to delaying the DQS signal by *about* 90 degrees is to allow for fine timing adjustments to the DQS signals by read leveling circuit 323 through a read leveling operation. *Id.* at 40 (citing Ex. 1005 ¶¶ 90–91, 140, Fig. 13; Ex. 1003 ¶¶ 137–138). Petitioner argues that read leveling in Hiraishi

includes performing a read operation which means that the amount of delay applied to the strobe signal DQS by delay circuit 372 would be based at least on signals received by the data buffer 300 during read leveling. *Id.* at 42–43 (citing Ex. 1005 ¶¶ 28, 140; Ex. 1003 ¶¶ 142–143).

Alternatively, with respect to the combination of Hiraishi and Butt, Petitioner argues that Butt discloses a delay circuit 104 that can delay read strobe signal DQS that is used to read data signal DQ. Pet. 44 (citing Ex. 1029 ¶¶ 17–18, Fig. 3A; Ex. 1003 ¶ 145). Petitioner argues that Butt describes a method of "read training" that can establish optimum DQS settings by adjusting a delay of the read data strobe signal DQS. *Id.* at 45 (citing Ex. 1029 ¶¶ 33, 35, Fig. 3A; Ex. 1003 ¶¶ 145–147). The optimum DQS settings established during read training are then used during later read operations, which Petitioner argues would teach one of skill in the art that Butt delays the data strobe signal by a predetermined amount based on signals received during a previous operation (i.e. the dummy data and strobe signals received during read training). *Id.* at 47 (citing Ex. 1003 ¶¶ 148, 150).

Petitioner argues that it would be been obvious to apply Butt's teachings to Hiraishi to set the delay for Hiraishi's delay circuit 372 by read leveling circuit 323 based on signals received during a prior read leveling process. Pet. 47 (citing Ex. 1003 ¶¶ 149–150). Hiraishi calls for read leveling and Butt teaches the details for performing read leveling. *Id.* According to Petitioner, "Butt provides the motivation: to 'enable[] a reliable data read operation for high speed applications."[4] *Id.* (emphasis

[4] Petitioner emphasizes, by underline, each instance of the names of the prior art references in its Petition. Unless otherwise noted, we omit these emphases in our quotations from the Petition.

omitted, alteration by Petitioner) (quoting Ex. 1029 ¶ 36). Petitioner also argues that a person of ordinary skill would have "had a reasonable expectation of success because the combination would be a simple application of known techniques to improve similar technology in a similar way, and Butt's calibration process 200 would offer the same benefit for Hiraishi's delay circuit 372 as for Butt." *Id.* at 47–48 (emphasis omitted) (citing Ex. 1003 ¶¶ 149–150).

Patent Owner argues that Petitioner fails to establish that Hiraishi alone or with Butt discloses a read strobe that is delayed based on signals received by the data buffer during a previous operation. Prelim. Resp. 30–43. With respect to Hiraishi alone, Patent Owner argues that, contrary to Petitioner's contentions, Hiraishi describes delaying the DQS signal by a fixed 90 degrees and that there is no teaching that Hiraishi's delay circuit 372 performs any fine timing adjustments to the DQS signal by the read leveling circuit. *Id.* at 31–32. This is because, according to Patent Owner, the delay circuit 372 is not disclosed as connected to any circuitry capable of providing any input that could alter the amount of delay applied by the delay circuit 372 to the DQS signal. *Id.* at 32–33 (citing Ex. 2005 ¶ 81); *see also id.* at 37–42 (explaining that none of the four outputs from read leveling circuit are used to adjust the delay of DQS by the delay circuit 372). Patent Owner argues that the JEDEC DDR standard allows for a delay tolerance which varies as a function of memory speed and that "Hiraishi's reference to 'about 90 degrees' is meant to reflect the imprecise nature of adding fixed amounts of delay to a DQS signal." *Id.* at 35 (citing Ex. 2005 ¶¶ 85–86; Ex. 2002, 81; Ex. 1019, 184–186; Ex. 1005 ¶ 91).

Addressing the combination of Hiraishi and Butt, Patent Owner argues that Butt cannot cure Hiraishi's deficiency because Hiraishi's read

leveling circuit is neither physically nor functionally connected to the delay circuit (as explained above) and the proposed combination with Butt does not change the manner in which the delay circuit is connected. Prelim. Resp. 43.

Patent Owner also argues that Petitioner fails to establish a motivation to combine Hiraishi with Butt. Prelim. Resp. 47–54. Specifically, Patent Owner argues Butt's approach for performing read leveling would render Hiraishi incapable of performing read leveling because Butt's read leveling approach requires DQ read data from the memory device but there is no evidence how Hiraishi's buffer could provide DQ read data from the memory to its leveling circuitry. *Id*. According to Patent Owner, the only input to delay circuit 372 is the DQS on terminal 351 or 352, and the only input to data register control circuit 320 is the DRC, and, thus, neither the delay circuit 372 nor data register control circuit 320 have access to the DQ read data. *Id*. at 51–52 (citing Ex. 2005 ¶¶ 100–101).

Patent Owner also argues that even if Hiraishi's read leveling could be replaced by Butt's strobe delay adjustment, one of ordinary skill would not have been motivated to do so. Prelim. Resp. 54–56. Petitioner relies on Butt's statement that its method would "enable[] a reliable data read operation for high speed applications." Ex. 1029 ¶ 36, *quoted in* Pet. 47. But according to Patent Owner, "Hiraishi already claims 'to realize a considerably high data transfer rate.'" *Id*. at 54 (citing Ex. 1005 ¶¶ 11, 69–70). Patent Owner argues "Petitioner does not explain or even suggest that the read leveling operation of Butt could make the read leveling operation in Hiraishi more reliable or otherwise better." *Id*.

At this stage of the proceeding, we determine Petitioner has established a reasonable likelihood that one of ordinary skill would have

combined Hiraishi and Butt in the manner proposed by Petitioner and that this combination teaches the limitations 1[f] and 1[i]. Petitioner supports its contentions with evidence from the relied upon references and from the testimony of Dr. Wedig as summarized above. Specifically, we are persuaded that the combination of Hiraishi and Butt teaches delaying a first read strobe by a first predetermined amount based on signals received in a previous operation. Hiraishi teaches a delay circuit 372 that delays data strobe signals, and Butt explicitly teaches "adjusting a delay of the read data strobe signal DQS to approximately center the read data strobe signal DQS in the valid data eye window" based on previously performed read training. Ex. 1005, ¶ 91, Fig. 5; Ex. 1029 ¶¶ 33–35.

We are also persuaded by Petitioner's arguments that there would be sufficient motivation to combine Hiraishi and Butt. Butt expressly states, in this regard, that its "invention generally enables a reliable data read operation for high speed applications." Ex. 1029 ¶ 36. Additionally, Dr. Wedig provides credible testimony that it would have been obvious to combine Hiraishi and Butt. Ex. 1003 ¶ 149. Specifically, Dr. Wedig testifies that a person of ordinary skill "would have recognized that the calibration provided by the read training in Butt would facilitate more accurate and rapid exchanges of data by centering the data strobe signal in a valid data eye." *Id*. (emphasis omitted).

Although Patent Owner argues that the combination would not successfully delay the read strobe signal based on previous operations due to Hiraishi's read leveling circuit not being connected to its delay circuit and due to the combination not providing DQ read data to delay circuit 372, at this stage of the proceeding we credit Dr. Wedig's testimony that a person of ordinary skill would have had a reasonable expectation of success in making

the combination. *Id*. For example, Dr. Wedig testifies that one of ordinary skill in the art would have been able to implement Butt's functionality in Hiraishi's delay circuit 372 and that doing so would be a simple application of known techniques to improve similar technology because Hiraishi's delay circuit 372 serves a function that is analogous to Butt's function of delaying the data strobe signal. *Id*.

c) Limitations 1[g] and 1[h]

Limitation 1[g] and 1[h] require the first data buffer is configurable to "sample the first section of the read data using the first delayed read strobe; and transmit the first section of the read data to a first section of the data bus." Ex. 1001, 19:49–52. Regarding limitation 1[g], Petitioner argues that the first data buffer is configurable to sample the first section of the read data using the first delayed read strobe. Pet. 36–38. Petitioner argues that one of ordinary skill would have understood that, "when the data signal is latched in the FIFO, it necessarily is sampled (registered) and, because the delayed DQS signal acts 'as an input trigger signal' to latch the data in the FIFO (Read) circuit 302, this is necessarily done in accordance with the delayed strobe signal received from delay circuit 372." Pet. 37 (citing Ex. 1003 ¶ 132; Ex. 1005 ¶ 91).

Petitioner argues, in the alternative, that if Hiraishi alone does not teach limitation 1[g], as explained above, then the combination of Hiraishi and Butt does. Pet. 37–38. According to Petitioner, Butt discloses a method for calibrating a delayed read strobe DQS such that "data is sampled using the delayed read data strobe signals DQS." *Id*. at 37 (citing Ex. 1029 ¶¶ 18, 35). Petitioner argues that Butt's sampling operation is equivalent to Hiraishi's use of the DQS signal to trigger the FIFO Read circuit 302. *Id*. at 37–38 (citing Ex. 1029 ¶ 19).

For limitation 1[h] Petitioner argues Hiraishi's data buffer transmits the first section of the read data DQ on data line L0 via terminal 340 to a first section of the data bus line 23. Pet. 38 (citing Ex. 1003 ¶¶ 134–135).

As to limitation 1[g] Patent Owner argues Petitioner has failed to establish Hiraishi alone samples read data using the delayed read strobe. Prelim. Resp. 43–47. Patent Owner argues that Hiraishi never mentions sampling read data using the delayed strobe provided by delay circuit 372. *Id.* at 43. Patent Owner takes issue with Petitioner's argument that when data is latched in the FIFO, it necessarily is sampled because Petitioner does not articulate any basis for this assertion or provide supporting citations. *Id.* at 44–45.

Patent Owner argues that the combination of Hiraishi and Butt also does not teach limitation 1[g]. This is because Butt is incompatible with Hiraishi. Prelim. Resp. 46. As Patent Owner explains, Butt discloses that the data is sampled before it is presented to the output FIFO while the alleged sampling in Hiraishi is performed during or after the data is presented to Hiraishi's FIFO Read circuit. *Id.* at 46 (citing Ex. 1029 ¶ 18). Thus, Patent Owner argues "incorporating Butt's method in Hiraishi would not arrive at the invention, or even an operable implementation, because Hiraishi does not have any circuitry that can sample data ***before*** FIFO 302, as required by Butt's method, and Petitioner has not explained how that could be done." *Id.* at 46.

Finally, Patent Owner argues Petitioner fails to present a prima facie case that a person of ordinary skill would have been motivated to modify Hiraishi with Butt's alleged sampling feature. Prelim. Resp. 56–58. Patent Owner points out that "[t]he only motivation provided is that '[t]he operation Butt describes as 'sampling' is ***equivalent*** to Hiraishi's use of the DQS

signal to trigger the FIFO (Read) circuit 302.'" *Id.* at 57 (alteration in original) (citing Pet. 37–38). However, according to Patent Owner, Petitioner does not explain why a person of ordinary skill would regard Butt's sampling as superior or preferable to Hiraishi's existing approach. *Id.* at 57.

At this stage of the proceeding, we determine Petitioner has established a reasonable likelihood that one of ordinary skill would have combined Hiraishi and Butt in the manner proposed by Petitioner and that this combination teaches the limitations 1[g] and 1[h]. Petitioner supports its contentions with evidence from the relied upon references and from the testimony of Dr. Wedig as summarized above. Specifically, we are persuaded that the combination of Hiraishi and Butt teaches sampling the first section of the read data using the first delayed read strobe. Butt expressly teaches that "[e]ach of the DPs 114 may be configured to present the DQ data to a respective asynchronous FIFO . . . after the data is sampled using the delayed read data strobe signals DQS." Ex. 1029 ¶ 18. We also agree with Petitioner's contention that Hiraishi transmits the first section of read data using the first delayed read strobe. *See* Ex. 1005, Fig. 5; Ex. 1003 ¶¶ 134–135.

As to Patent Owner's argument that Butt is incompatible with Hiraishi because in Butt the data is sampled before it is presented to the FIFO while in Hiraishi the data is sampled during or after the data is presented to Hiraishi's FIFO Read circuit, at this stage of the proceeding we determine that the one of ordinary skill in the art would have understood how to make the combination with a reasonable expectation of success, as supported by Dr. Wedig's testimony. *See* Ex. 1003 ¶¶ 133, 149. We are also persuaded by Petitioner's argument that one of ordinary skill would have been

sufficiently motivated to combine Butt with Hiraishi because Butt describes a method that enables a reliable data read operation for high speed applications. Ex. 1029 ¶ 36.

d) Conclusion as to Claim 1

For the aforementioned reasons we are persuaded that the combination of the Hiraishi and Butt teaches the limitations of claim 1 and that Petitioner has established a reasonable likelihood that the combination would have rendered claim 1 obvious.

4. Analysis of Claims 2, 4, 6, 7, 11, 13–15, 17, and 18

Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing of a reasonable likelihood that claims 2, 4, 6, 7, 11, 13–15, 17, and 18 would have been obvious over the combination of Hiraishi and Butt. *See* Pet. 48–68. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See* Prelim. Resp.

5. Conclusion – Obviousness over Hiraishi and Butt (Ground 1)

Accordingly, having considered the arguments and evidence, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 of the '506 patent as obvious over Hiraishi and Butt.

E. Obviousness over Hiraishi, Butt, and Tokuhiro (Ground 4)

Petitioner argues claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 of the '506 patent would have been obvious over Hiraishi, Butt, and Tokuhiro. Pet. 93–125. Below we provide a brief overview of Tokuhiro and then analyze Petitioner's contentions in light of Patent Owner's arguments.

1. Tokuhiro (Ex. 1006)

Tokuhiro relates to a memory control circuit having "a write leveling function and control[ing] read/write operations by supplying a clock signal to a plurality of memories." Ex. 1006, 3:16–20. Tokuhiro explains that, in memory interfaces, "a propagation delay is generated" because a "clock signal CK output from [a] memory controller 90 cannot reach all the [memory units] at the same time." *Id.* at 1:63–2:1. Tokuhiro further explains that delay is addressed through a write leveling function for "adjusting (compensating) a delay time" of "data strobe signal DQS." *Id.* at 2:10–18. For its write level technique, Tokuhiro describes "delaying, in [a] write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time." *Id.* at 3:16–26.

In one example, "during the write operation, [a] first variable delay circuit DW delays the data strobe signal DQS output to the SDRAM by the first delay time Dt1 that has been set based on the write leveling function." Ex. 1006, 14:66–15:2. Tokuhiro explains that a "delay time . . . calculated is provided as Delay (R)n. In other words, the second delay time Dt2 for the data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling." *Id.* at 16:19–23; *see id.* 16:1–18.

2. Petitioner's Proposed Combination and Reasons to Combine

Petitioner relies on Tokuhiro for its ability to delay transmission of read data based on a delay time determined during a write operation. Pet. 94. Petitioner proposes to implement the functionality of the delay

elements (DR) of Tokuhiro in the data buffers of Hiraishi. *Id*. at 103–111. Specifically, Petitioner proposes to add Tokuhiro's read delay elements (e.g. DR-1) to Hiraishi's data register buffer immediately after the read data from the memory is latched in Hiraishi's FIFO Read Circuit 302. *Id*. at 107–109. Alternatively, Petitioner argues that Tokuhiro's delay elements could be used instead of Hiraishi's FIFO circuit for delaying read data. *Id*. at 110. Petitioner presents two different implementations of the Hiraishi, Butt, and Tokuhiro combination. The first being where the system memory controller determines the read delay. *Id*. at 112–113. The second is where the module controller determines the read delay. *Id*. at 114–119.

Petitioner provides three motivations to combine Tokuhiro with Hiraishi, including that (1) Tokuhiro teaches calculating read delays based on the delays for write operations, which is more efficient than Hiraishi's technique of performing read leveling independent of write delays; (2) Tokuhiro provides simple techniques for removing fly-by delays, while Hiraishi does not disclose how its memory controller re-times read data received with fly-by delays; and (3) Tokuhiro discloses simple solutions for fly-by delays greater than one clock cycle, while Hiraishi does not. Pet. 95–103.

Patent Owner argues that although Petitioner relies on the combination of Hiraishi, Butt, and Tokuhiro, "each of the alleged motivations to combine . . . is directed to a proposed modification of only an ***unmodified*** Hiraishi with Tokuhiro, not to a proposed ***further*** modification of a Hiraishi-Butt combination with Tokuhiro." Prelim. Resp. 59.

Patent Owner further argues that Petitioner does not explain how adding Tokuhiro's delay element DR-1 reconciles with the delayed strobe provided by the delay circuit 372 which, Patent Owner argues, is delayed by

a significant 90-degrees. Prelim. Resp. 62. Patent Owner argues that Petitioner's combination cannot account for the delay introduced by delay circuit 372 because the delay from this circuit is not an input to Tokuhiro's DR-1 delay element in Petitioner's proposed combination. *Id*. at 62–63.

Patent Owner argues, with respect to Petitioner's first implementation in which the system memory controller determines the read delay (Pet. 112–113), that a person of ordinary skill in the art would not have implemented Hiraishi's S5 leveling operations to program the read delay elements added from Tokuhiro to Hiraishi's data buffer. Prelim. Resp. 64–68. This is because Hiraishi's S5 leveling accounts only for delays between the system memory controller and the data buffers, not between the data buffers and the memory devices, the latter of which, Patent Owner argues, is what the claims of the '506 patent are directed to. *Id*. at 66–67. Patent Owner also argues that Petitioner fails to establish that the first implementation would be operable because Tokuhiro's read and write leveling are performed by the computer's main CPU, not its memory controller. *Id*. at 68. According to Patent Owner, in Tokuhiro, the delay elements are connected over dedicated CPU control lines on which control signals are provided, whereas in Petitioner's proposed combination, the only inputs to delay element DR-1 are the DQS signal and the local clock signal and no evidence has been presented that the components can be modified to operate in the proposed combination. *Id*. at 71–72.

With respect to the second implementation, Patent Owner argues that Petitioner failed to identify what component in Hiraishi the module controller is and that, because of this, it is impossible to discern what the basis for Petitioner's second implementation is. Prelim. Resp. 77–78. Further, Patent Owner argues that the Petition does not identify any passage

of Hiraishi that suggests that the functionality of its memory controller can be implemented by its data register buffers, as contended by Petitioner. *Id.* at 79. Moreover, according to Patent Owner, the functionality relied on by Petitioner is implemented by Tokuhiro's main CPU, not the memory controller and thus Petitioner's motivation for the second implementation fails. *Id.* at 79–80. Finally, Patent Owner argues that although the second implementation relies on Hiraishi's time measurement technique to measure time intervals to determine the corresponding fly-by-delay, what the Petition describes is the idea of determining the time delay between the memory controller and the data register buffer, not between the data register buffer and the memory devices. *Id.* at 80.

At this stage of the proceeding, we determine Petitioner has provided a sufficient reason to combine Hiraishi, Butt, and Tokuhiro. For example, Petitioner argues that Tokuhiro's method of calculating read delays based on the delays for write operations is more efficient than Hiraishi's technique of performing read leveling independent of write delays. Pet. 95–99 (citing Ex. 1003 ¶¶ 279–288). Petitioner also argues Tokuhiro provides techniques to remove fly-by delay while Hiraishi does not disclose how its memory controller re-times read data received with fly-by delays. Pet. 100 (citing Ex. 1003 ¶¶ 289–292). Petitioner argues that Tokuhiro discloses simple solutions for fly-by delays greater than one clock cycle, while Hiraishi does not. Pet. 101–103 (citing Ex. 1003 ¶¶ 293–299). Petitioner supports its contentions with credible testimony from Dr. Wedig who testifies that performing the write and read leveling operations of Hiraishi would require circuitry in both the data register buffer and the memory controller but that this circuitry could be simplified by implementing Tokuhiro's technique of setting read delays based on write delays. Ex. 1003 ¶¶ 283–288. Dr. Wedig

also testifies that Tokuhiro teaches that problems arise if fly-by delays on read operations are not compensated, especially if such delays exceed the clock period, and also teaches solutions to this problem. Ex. 1003 ¶¶ 293–299.

As summarized above, Patent Owner makes various arguments why one of ordinary skill would not have been motivated to combine Tokuhiro with Hiraishi and why the proposed combination would not have been operable or would have required further modification that Petitioner has not described. At this stage of the proceeding we determine Petitioner has presented sufficient evidence and reasoning supporting its proposed combination and explaining why one of ordinary skill in the art would have combined the references in the manner proposed. For example, Dr. Wedig testifies that it would have been obvious to implement Tokuhiro's delay elements in Hiraishi's data register buffers in the manner described by Petitioner, for example by applying the read delay immediately after the read data from the memory is latched. Ex. 1003 ¶¶ 300–321. Dr. Wedig also testifies that when Tokuhiro's read delay elements are added to Hiraishi's data buffer, existing delay circuit 372 would still continue to make fine timing adjustments to the phase of the strobe DQS. *Id.* ¶ 304. This testimony supports Petitioner's arguments that one of ordinary skill would have had a reasonable expectation of success in making the combination. While Patent Owner presents multiple arguments to the contrary, with support from the testimony of Dr. Khatri, we determine that the weight of Petitioner's evidence is sufficient at this stage of the proceeding.

3. Analysis of Claim 1

Petitioner relies on the same contentions made in Ground 1, over Hiraishi and Butt, for all limitations of claim 1 except limitations 1[f] and

1[i]. Pet. 119–120. Our analysis of Ground 1 above, therefore, applies for those limitations where they are applicable and will not be repeated here.

As a reminder, limitations 1[f] and 1[i] require that in response to one or more of the module control signals, the first data buffer is configurable to: 1[f] "delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;" 1[i] "wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations." Ex. 1001, 19:44–55. Petitioner argues that Tokuhiro's delay element DR-1 added to Hiraishi's data buffer circuit would delay the strobe signal from selector 332 and provide that delayed strobe signal to the FIFO Read Circuit 302. Pet. 120 (citing Ex. 103 ¶ 323). The delay introduced by Tokuhiro's DR-1 delay element for the read operation would be based on an earlier write operation, according to Petitioner. *Id.* at 121–122 (citing Ex. 1006, 18:53–63, 2:13–18).

At this stage of the proceeding we are persuaded by Petitioner's arguments which we determine are supported by disclosures from Hiraishi, Butt, and Tokuhiro and by Dr. Wedig's testimony. Patent Owner does not make separate arguments, in addition to those discussed above, regarding these limitations.

a) Conclusion as to Claim 1

For the aforementioned reasons, we are persuaded that the combination of Hiraishi, Butt, and Tokuhiro teaches the limitations of claim 1 and that Petitioner has established a reasonable likelihood that the combination would have rendered claim 1 obvious.

4. Claims 2, 4, 6, 7, 11, 13–15, 17, and 18

Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing of a reasonable likelihood that

claims 2, 4, 6, 7, 11, 13–15, 17, and 18 would have been obvious over the combination of Hiraishi and Butt. *See* Pet. 122–125. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See* Prelim. Resp.

5. Conclusion – Obviousness over Hiraishi, Butt, and Tokuhiro (Ground 4)

Accordingly, having considered the arguments and evidence, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1, 2, 4, 6, 7, 11, 13–15, 17, and 18 of the '506 patent as obvious over Hiraishi, Butt, and Tokuhiro.

F. Obviousness over Hiraishi, Butt, and Ellsberry (Ground 2); Obviousness over Hiraishi, Butt, and Kim (Ground 3); Obviousness over Hiraishi, Butt, Tokuhiro, and Ellsberry (Ground 5); Obviousness over Hiraishi, Butt, Tokuhiro, and Kim (Ground 6)

Petitioner argues that claims 3, 5, 12, and 16 of the '506 patent would have been obvious over Hiraishi, Butt, and Ellsberry (Pet. 68–78); that claims 8–10, 19, and 20 of the '506 patent would have been obvious over Hiraishi, Butt, and Kim (*id*. at 79–93); that claims 3, 5, 12, and 16 of the '506 patent would have been obvious over Hiraishi, Butt, Tokuhiro, and Ellsberry (*id*. at 126–127); and that claims 8–10, 19, and 20 of the '506 patent would have been obvious over Hiraishi, Butt, Tokuhiro, and Kim (*id*. at 127).

Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing of a reasonable likelihood that the challenged claims under the aforementioned grounds would have obvious over the respective references. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See* Prelim. Resp.

III. CONCLUSION

Petitioner has demonstrated a reasonable likelihood of prevailing in showing the unpatentability of at least one challenged claim of the '506 patent. At this stage of the proceeding, however, we have not made a final determination with respect to the patentability of the challenged claims.

IV. ORDER

For the foregoing reasons, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–20 of the '506 patent is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '506 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

IPR2022-00711
Patent 10,860,506 B2

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Paper: 15
Entered: October 19, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00639
Patent 10,949,339 B2

Before JON M. JURGOVAN, DANIEL R. GALLIGAN, and NABEEL U. KHAN, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–35 of U.S. Patent No. 10,949,339 B2 (Ex. 1001, "the '339 patent"). Paper 1 ("Pet."), 1. Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp."). Petitioner filed an authorized Preliminary Reply (Paper 13) ("Reply"), and Patent Owner filed an authorized Preliminary Sur-Reply (Paper 14) ("Sur-Reply").

We have jurisdiction and authority to institute trial pursuant to 35 U.S.C. §§ 6 and 314(a), and 37 C.F.R. § 42.4(a). Upon consideration of the Petition, Preliminary Response, Reply, and Sur-Reply, we institute *inter partes* review under § 314(a).

II. BACKGROUND

A. Real Parties-in-Interest

Petitioner identifies itself and Samsung Semiconductor, Inc. as the real parties-in-interest involved in this case. Pet. xxxii. Patent Owner identifies itself as the real party-in-interest in this case. Paper 3, 1.

B. Related Matters

Petitioner and Patent Owner identify the following as matters that can affect or be affected by this proceeding. *See* Pet. xxxii– xxxiii; Paper 3, 1.

- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, 1:21–cv-01453 (D.Del. Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021
- U.S. Application No. 16/841,552 (abandoned)
- U.S. Application No. 17/202,021

- IPR2017-00577 (U.S. Patent No. 8,516,185
- IPR2018-00362 (U.S. Patent No. 9,606,907)
- IPR2018-00363 (U.S. Patent No. 9,606,907)
- IPR2018-00364 (U.S. Patent No. 9,606,907)
- IPR2018-00365 (U.S. Patent No. 9,606,907)
- *In the Matter of Certain Memory Modules and Components Thereof*, Inv. No. 337-TA-1089 (USITC filed Oct. 31, 2017) (U.S. Patent No. 9,606,907)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016) (U.S. Patent No. 8,516,185)

C. Overview of the '339 Patent

The '339 patent is titled "Memory Module with Controlled Byte-Wise Buffers." Ex. 1001, code (54). The memory module communicates with a memory controller and comprises double data rate (DDR) dynamic random access memory (DRAM) devices arranged in multiple ranks each of the same width as the memory module. *Id.* at code (57). The module controller is configured to receive and register input control signals for a read or write operation from the memory controller and to output registered address and control signals to the DRAM devices. *Id.* The memory module further comprises byte-wise buffers controlled by a set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank. *Id.*

Figure 3C of the '339 patent is shown below.

Figure 3C:

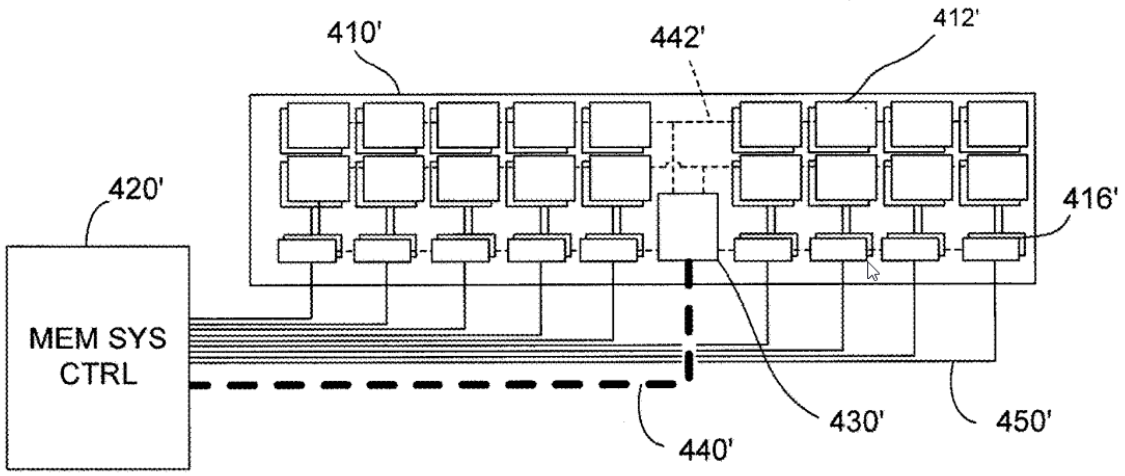

Figure 3C shows a layout of memory devices 412', data transmission circuits 416', and control circuit 430' on printed circuit board (PCB) 410' of memory module 402'. Ex. 1001, 3:57–60, 9:10–13. Memory devices 412' are arranged in ranks on PCB 410'. *Id.* at 9:27–31. Memory devices 412' are connected to data transmission circuits 416' arranged along the bottom edge of memory module 410'. *Id.* at 9:18–26. Data transmission circuits 416' are further connected to memory control system 420' via data lines 450'. *Id.* at 7:59–61. Memory system controller 420' connects to control circuit 430' via address and control lines 440'. *Id.* at 7:64–65. Control circuit 430' in turn connects with memory devices 412' via lines 442'. *Id.* at 10:17–21. Control circuit 430' receives commands and address signals from memory system controller 420' and generates appropriate control and address signals to select memory devices 412' and carry out the command (e.g., a read or write operation). *Id.* at 7:56–58, 8:23–26, 10:33–50.

Figure 5 of the '339 patent is shown below.

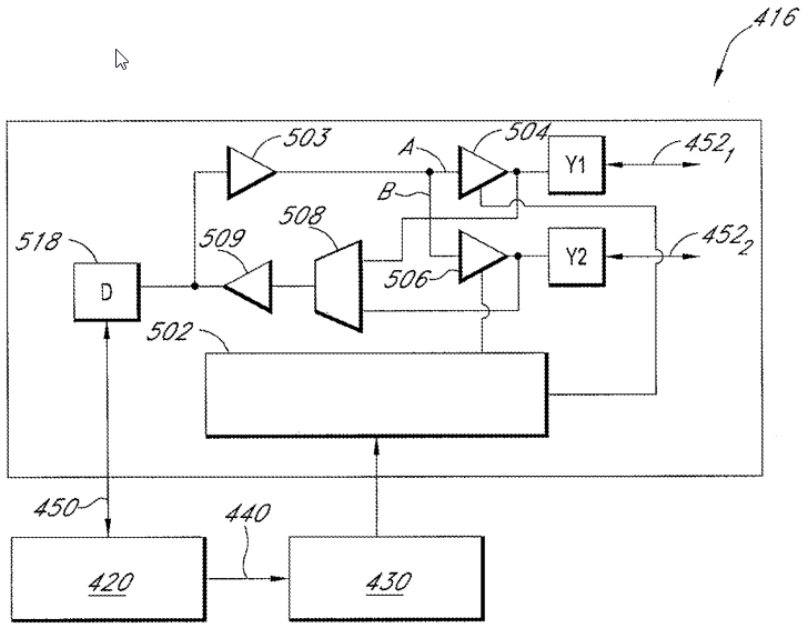

FIG. 5

Figure 5 shows a data transmission circuit 416. *Id.* at 4:4–6. Data transmission circuit 416 includes control logic circuitry 502 to control various components including buffers, switches, and multiplexers. *Id.* at 15:26–33. The embodiment of Figure 5 is 1-bit wide and switches a single data line 518 between the memory controller 420 and memory devices 412. *Id.* at 15:33–35. In a write operation, data entering data line 518 is driven onto two data paths, labeled path A and path B after passing through write buffer 503. *Id.* at 15:45–48. Ranks of memory devices 412 are divided into groups in ranks A and C associated with path A, and ranks B and D, associated with path B. *Id.* at 15:48–58. Control circuit 430 provides enable control signals to control logic circuitry 502 to select either path A or B to direct the data. *Id.* at 16:7–11. First tri-state buffer 504 in path A is enabled, and second tristate buffer in path B is disabled with its output in a high-impedance condition. *Id.* at 16:13–16. Data is directed along path A to

terminal Y1 connected to the first group of memory devices 412, ranks A and C. *Id.* at 16:16–20. If an "enable B" signal is received, then first tristate buffer 504 opens path A and the second tristate buffer 504 closes path B, thus directing the data to second terminal Y2 that is connected to the second group of memory devices 412 in ranks B and D. *Id.* at 16:21–25.

D. Illustrative Claim

Claims 1, 11, 19, and 27 are independent claims and the rest are dependent. Claim 1, reproduced below, is illustrative of the claimed invention:

> [1pre] A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:
>
> [1a] a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket;
>
> [1b] double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks;
>
> [1c1] a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first Nbit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals,
>
> [1c2] wherein the registered address and control signals cause

the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals; and

[1d1] a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals

[1d2] wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side,

[1d3] wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;

[1e] wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and

[1f] wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

Ex. 1001, 19:9–67.

E. Evidence [1]

Reference		Date	Exhibit No.
Ellsberry[2]	US 2006/0277355 A1	Dec. 7, 2006	1005
Halbert[3]	US 7,024,518 B2	Apr. 4, 2006	1006

Pet. 1, 11–13.

F. Asserted Challenges to Patentability

Claim Challenged	35 U.S.C. §	Reference(s)/Basis
1–35	§ 103(a)	Ellsberry, Halbert

Pet. 1.

III. ANALYSIS

A. Discretionary Denial Under 35 U.S.C. § 325(d)

Under § 325(d), in determining whether to institute an *inter partes* review, "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." In evaluating arguments under § 325(d), we use a two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or

[1] Petitioner also relies upon the Declaration of Dr. Vivek Subramanian (Ex. 1003).

[2] Petitioner contends Ellsberry is prior art under pre-AIA 35 U.S.C. § 102(b). Pet. 11.

[3] Petitioner contends Halbert is prior art under pre-AIA 35 U.S.C. § 102(b). Pet. 12.

whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"). We also consider the non-exclusive factors set forth in *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential in relevant part) ("*Becton, Dickinson*"), which "provide useful insight into how to apply the framework" under § 325(d). *Advanced Bionics* at 9. Those non-exclusive factors are the following:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;
>
> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
>
> (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
>
> (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson at 17–18. "If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office, then factors (c), (e), and (f) relate to

whether the petitioner has demonstrated a material error by the Office." *Advanced Bionics* at 10.

1. Advanced Bionics Part 1

Turning to the first part of the *Advanced Bionics* framework, we consider whether the same or substantially the same art or arguments previously were presented to the Office.

The record shows that the Examiner considered Ellsberry during examination of the '339 patent. Ex. 1001, 2; Ex. 1002, 233, 314–357, 396, 518, 520, 521, 547–594, 650–655, 664, 677–682, 687–735, 803–808, 813, 832–837, 852, 854. The record likewise shows that the Examiner considered Halbert during examination of the '339 patent. Ex. 1001, 2; Ex. 1002, 147, 151, 155, 196, 197, 233, 312, 346, 348, 350, 352, 354–357, 396, 518, 519, 548, 582–587, 589, 591, 593, 650, 677, 687, 721, 723, 725–730, 732, 734, 803, 832. Furthermore, for IPR2018-00362, Paper 29 ("Termination Decision Document") is listed on the '339 patent as having been considered by the Examiner. Ex. 1001, 9. In IPR2018-00362, Ellsberry and Halbert were asserted against U.S. Patent 9,606,907 B2 (the '907 patent), which is the parent of the '339 patent.

Thus, under the first part of *Advanced Bionics*, we find that same or substantially the same art or arguments previously were presented to the Office regarding Ellsberry and Halbert.

2. Advanced Bionics Part 2

Under the second part of the *Advanced Bionics* framework, we consider whether Petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims.

Petitioner contends that the Examiner erred by not considering the combination of Ellsberry and Halbert. Pet. 145. We agree. Although the

Examiner considered Ellsberry and Halbert individually during examination, we find no evidence that the Examiner considered them together for Ellsberry's teachings of rank-multiplied memory module with tristate buffers, load isolation, and CAS latency, and Halbert's teaching of tristate buffers to buffer data in memory modules in a context similar to the '339 patent. *See* Pet. 146–148 (comparing Ex. 1001, Figs. 4, 5 with Ex. 1006, Fig. 4). Consequently, we find the Examiner erred in a manner material to patentability of the '339 patent's claims.

Petitioner also contends that during prosecution the Examiner correctly rejected the '339 patent's claims as "'not patentably distinct' from various claims of the '907 Patent." Pet. 148–149 (citing Ex. 1002, 144–152). The '907 patent is the parent of the '339 patent. Pet. 41; Ex. 1001, code (63). To overcome this rejection, Patent Owner filed terminal disclaimers. *Id.* (citing Ex. 1002, 196–197, 213, 497–503, 519).

Petitioner contends that the Examiner erred by not addressing the Board's Final Written Decision in IPR2018-00362, Paper 29, finding claims of the '907 patent unpatentable after finding the '339 patent claims patentably indistinct. We agree. A patent owner or applicant is precluded from obtaining "a claim that is not patentably distinct from a finally refused or canceled claim." 37 C.F.R. § 42.73(d)(3)(i). The Examiner should have considered the impact of the Board's Final Written Decision on the patentably indistinct claims sought by Patent Owner. Since there is no evidence in the record the Examiner so considered the claims, we find the Examiner erred in a manner material to patentability of the claims.

Patent Owner argues that the '339 patent's claims were substantially amended after the terminal disclaimers were filed such that they were patentably distinct from the '907 patent. Prelim. Resp. 77. We find no

evidence, however, that Patent Owner made any effort to withdraw the terminal disclaimers due to the amended claims being patentability distinct from those of the '907 patent. *See* Ex. 1002. In addition, Petitioner points to at least one example where Patent Owner amended the claims but allegedly did not change the substance of the limitation. Pet. 42; Reply 3–4. No showing has been made here that the claims of the '339 patent were substantively amended to be patentably distinct from the '907 patent's claims.

We decline to exercise our discretion to deny institution of *inter partes* review under § 325(d). Accordingly, we proceed to the merits of Petitioner's obviousness contentions.

B. Obviousness Challenges

1. Principles of the Law of Obviousness

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results.[4] *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

[4] The parties do not identify any evidence secondary consideration of nonobviousness.

When evaluating a combination of teachings, we must also "determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). "[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Kahn*, 441 F.3d at 988.

2. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). "Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case." *Id.*

Petitioner contends that a person of ordinary skill in the art in the field of the '339 patent in 2009 would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Pet. 2 (citing Ex. 1003 ¶¶ 50–51). Petitioner contends such person would have been familiar with various standards of the day including JEDEC industry standards, knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id.*

For purposes of its Preliminary Response only, Patent Owner applies the skill level of a POSITA proposed by Petitioner. Prelim. Resp. 28.

On this record, we accept Petitioner's statement of the level of ordinary skill in the art except that we omit the qualifiers "at least" before years of education and experience because they render the level ambiguous and encompass levels that are beyond ordinary. Otherwise, we find Petitioner's statement of the level of ordinary skill in the art consistent with the '339 patent and the applied prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

3. Claim Construction

We construe claim terms "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2019). There is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the specification. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Nonetheless, if the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor's lexicography governs." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing Phillips, 415 F.3d at 1312–17). Only

disputed claim terms must be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner discusses the terms "rank" and "rank select signal" in the claim construction section of its Petition. Pet. 8–10. Patent Owner contends that Petitioner does not offer any actual proposed construction for these terms, so there is no need to construe them. Prelim. Resp. 27. As there is no evidence of any dispute concerning these terms, we decline to construe them. *See Nidec, supra*.

Petitioner also contends that the '339 patent pertains to "fork in the road" configuration as opposed to a "straight line" configuration. Pet. 10–11. Petitioner does not show how its "fork in the road" configuration relates to any term in the '339 patent's claims. *Id.* Accordingly, we agree with Patent Owner there is no need to construe any term. Prelim. Resp. 27.

4. Ellsberry (Ex. 1005)

Ellsberry is titled "Capacity-Expanding Memory Device." Ex. 1005, code (54). "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch." *Id.* "By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry is shown below.

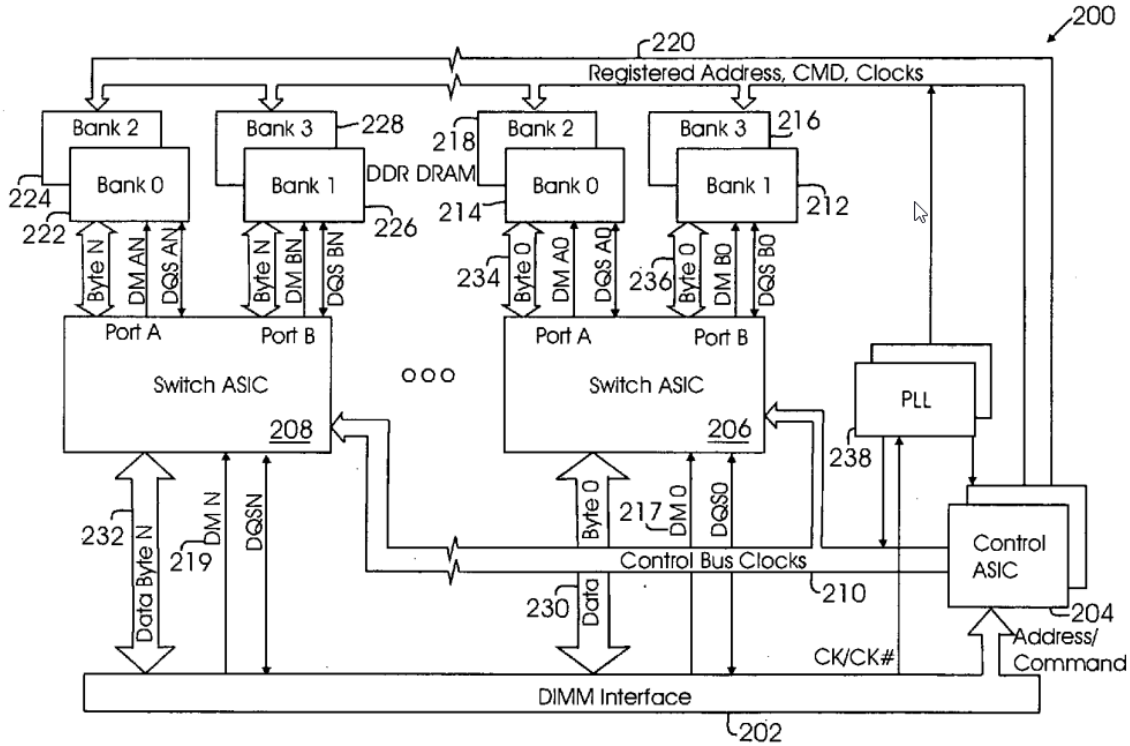

Fig. 2

Figure 2 "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." *Id.* ¶ 28. In Figure 2, system 200 has a DIMM interface 202 that couples to a "memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." *Id.* "The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206 & 208." *Id.* Figure 2 of Ellsberry illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202 and generates corresponding control signals on bus 210 and addresses on bus 220 to selectively connect memory banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. *Id.* ¶¶ 28–29. Ellsberry also teaches that the command scheme for a control unit operating multiple banks includes a CAS_n parameter pertaining to latency. *Id.* ¶ 19, Fig. 8B, n.3.

5. Halbert (Ex. 1006)

Halbert is titled "Dual-Port Buffer-to-Memory Interface" and teaches a memory module with selectable ranks of memory devices. Ex. 1006, codes (54), (57). Halbert's Figure 4 is shown below.

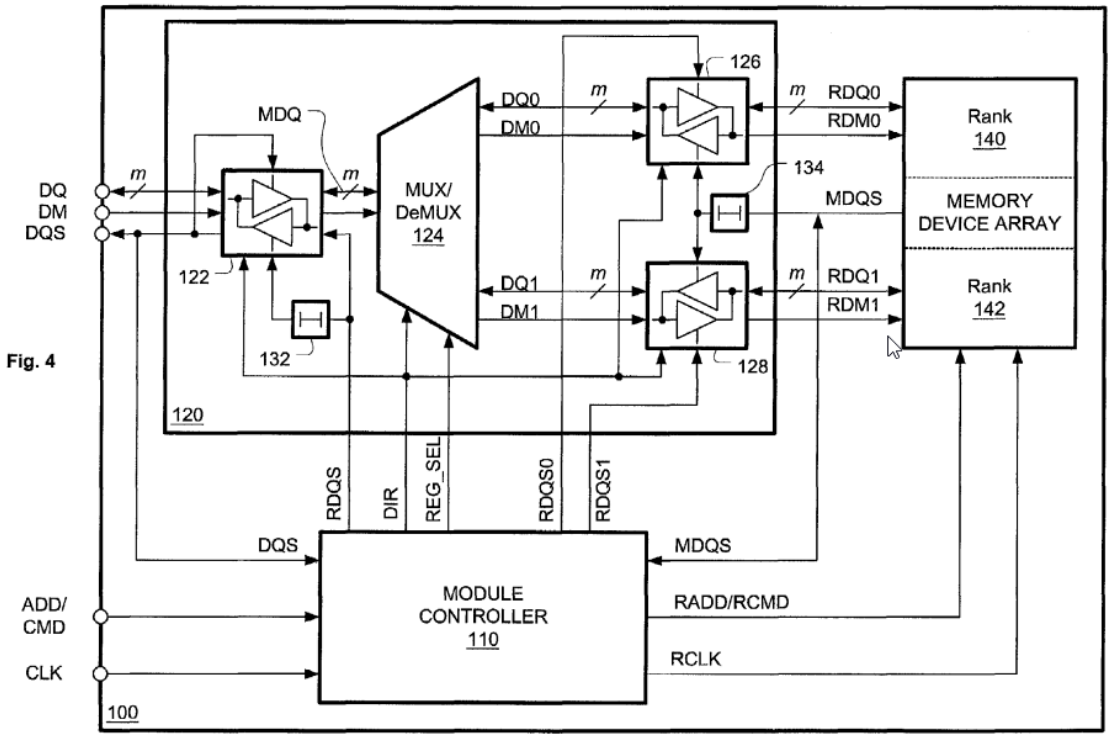

Fig. 4

In Figure 4, memory module 100 includes a module controller 110; data interface circuit 120; and a memory device array 140/142. *Id.* at 4:36–39. Module controller 110 synchronizes operation of module 100 with the attached memory system. *Id.* at 4:40–41. Module controller 110 also provides timing and synchronization signals to data interface circuit 120. *Id.* at 4:45–47. Data interface circuit 120 provides for m-bit-wide data transfers between the memory module and the system memory data bus, and Rxm-bit-wide data transfers between the interface circuit and the memory device array. *Id.* at 4:49–53. In Figure 4, R is 2 because the memory device array

comprises two ranks 140 and 142, each capable of performing m-bit-wide data transfers. *Id.* at 4:52–55.

Bidirectional buffer 122 is coupled to a bi-directional module data port that can be connected to a system memory data bus. *Id.* at 4:60–62. An m-bit wide path through buffer 122 receives and drives data signals DQ on the system memory data bus. *Id.* at 4:62–64. Two bi-directional data registers 126 and 128 connect, respectively, to memory device array ranks 140 and 142. *Id.* at 5:6–7. Each data register can drive an m-bit-wide word to that rank. *Id.* at 5:8–11.

Multiplexer/demultiplexer 124 multiplexes data signals DQ0 from register 126 and DQ1 from register DQ1 to buffer 122 when the module is reading from memory device array 140/142. *Id.* at 5:15–19. When the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1. *Id.* at 5:20–22.

Module controller 110 synchronizes operation of the data port buffer 122, MUX/deMUX 124, and data registers 126 and 128 via control signals. *Id.* at 5:23–25. Buffers 122, 126, and 128 are illustrated as bidirectional tristate buffers.

6. Motivation to Combine Ellsberry and Halbert

Petitioner contends that one of ordinary skill in the art would have been led to combine Ellsberry and Halbert. Pet. 44–47. Petitioner contends Halbert and Ellsberry are analogous because they are directed to improving memory modules, and have three bi-directional data buses in a "fork-in-the-road" layout and are directed to presenting a single load to the memory system rather than the loads of multiple ranks of memory devices. *Id.* (citing Ex. 1005 ¶¶ 6–9, 12, 45, Fig. 4; Ex. 1006, 3:67–4:5, 4:18–22, Fig. 4; Ex. 1001, 4:27–47, Fig. 5; Ex. 1003 ¶ 264). Petitioner contends one of

ordinary skill in the art would have considered it obvious to implement Ellsberry's bidirectional drivers with Halbert's tristate buffers to interface with each of the three bidirectional busses as taught by Halbert to eliminate bus conflicts in accordance with standard protocols and to present a single load to the system memory controller. *Id.* at 46 (citing Ex. 1003 ¶¶ 257–264). According to Petitioner, adding such a bidirectional buffer to interface the system memory bus and implementing Ellsberry's bidirectional drivers with tristate buffers would have been well within the level of skill at the time, since both Ellsberry and Halbert teach using bidirectional buffers interfacing with bidirectional busses as taught in textbooks for decades. *Id.* at 46–47 (citing Ex. 1005 ¶ 45, Fig. 4; Ex. 1006, 5:23–65, 9:27–35, Fig. 4; Ex. 1035, 133, Fig. 4.7; Ex. 1003 ¶¶ 261–263). Petitioner contends that the combination of Ellsberry and Halbert would have provided nothing more than expected at the time: lowering the load seen by the system data bus 230 to a single load and providing an operational interface to bidirectional data busses 234 and 236. *Id.* at 47 (citing Ex. 1003 ¶ 264).

Patent Owner argues that Ellsberry's memory bank switches already present a single load to the bus and that Petitioner's proposed modification performs a redundant function. Prelim. Resp. 4. Patent Owner further contends that Halbert's and Ellsberry's architectures are incompatible and that there is no competent evidence that tristate buffers would avoid bus conflicts. Prelim. Resp. 30–31, 48–49, 53–57; Sur-Reply 3; Ex. 2001 ¶¶ 82–84.

We determine that Petitioner provides sufficient evidence of a motivation to combine Ellsberry and Halbert. Petitioner shows sufficiently that Halbert's tristate buffers would improve Ellsberry's bidirectional drivers by providing a high-impedance state effective for isolating loads. Pet. 46

(citing Ex. 1003 ¶¶ 257–264). Use of a known technique to improve similar devices in the same way has been recognized as a proper motivation to combine. *See KSR*, 550 U.S. at 417. Alternatively, the combination may be viewed as the simple substitution of one known element for another, which is another recognized motivation to combine. *Id.*

Although Patent Owner contends that Ellsberry's data buffers and Halbert's tristate buffers provide redundant functions, that is not entirely correct. Bidirectional tristate buffers provide a high-impedance state on both sides of a buffer. *See* Ex. 1035, 68, 74 (Fig. 2.28), 117. Petitioner has provided sufficient evidence that bidirectional tristate buffers would be effective in eliminating bus conflicts if driven appropriately by a controller. Pet. 46–47; Ex. 1003 ¶¶ 256–265, 374. Accordingly, we determine that Petitioner shows sufficiently that one of ordinary skill in the art would have been motivated to combine Ellsberry and Halbert.

7. Claim 1

Petitioner contends that claim 1 of the '339 patent is unpatentable over the combination of Ellsberry and Halbert. Pet. 47–86. The preamble of claim 1 recites:

> [1pre] A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:

Ex. 1001, 19:9–15. Petitioner contends that Ellsberry teaches an N-bit wide memory module 106 mountable via DIMM interface 202 in a memory socket of computer system 100, which is configured to communicate address and control signals with processing unit 102 via communication path 110.

Pet. 47–48 (citing Ex. 1005, Figs. 1–3, 5, 6). Petitioner contends that Ellsberry teaches that the N-bit with data signal lines include sets of data signal lines (9 sets) with each set a byte wide (8 bits). *Id.* at 48–49 (citing Ex. 1005 ¶¶ 2, 3, 11, 14, 23, 26–30, 34, Figs. 1, 2 (data buses 230, 232), 5, 6; Ex. 1003 ¶¶ 267–278). Petitioner has shown sufficiently that Ellsberry teaches the preamble limitation [1pre] of claim 1.

Limitation [1a] of claim 1 of the '339 patent recites "a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket." Ex. 1001, 19:16–20. Petitioner contends that Ellsberry alone or with Halbert teaches the claimed PCB. Pet. 49–51 (citing Ex. 1003 ¶¶ 279–295). Specifically, Petitioner contends that Ellsberry teaches a substrate 502/602 with an edge interface 506. Pet. 49 (citing Ex. 1005 ¶¶ 2, 21, 27, 28, 47, 50, claim 10, Figs. 5, 6). Petitioner also contends that Halbert teaches that its DIMM is a circuit board with an edge connector with contacts releasably connecting to corresponding contacts of a memory socket. Pet. 50–51 (citing Ex. 1006, 2:3–14, Figs. 1, 8; Ex. 1003 ¶¶ 288–295). Petitioner has shown sufficiently that Ellsberry alone and with Halbert teach limitation [1a] of claim 1.

Limitation [1b] of claim 1 of the '339 patent recites "double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks." Ex. 1001, 19:21–23. Petitioner contends that Ellsberry discloses DDR DRAM devices 512 coupled to substrate 502/602 that are arranged in nine 8-bit memory devices, or nine pairs of 4-bit memory devices. Pet. 51–54 (citing Ex. 1005 ¶¶ 3, 26, 30–32, 40, 46, 47, Figs. 2, 5, 6, 11, 13; Ex. 1003 ¶¶ 296–305). Petitioner has shown

sufficiently that Ellsberry teaches limitation [1b] of claim 1.

Limitation [1c1] of claim 1 of the '339 patent recites

> a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals.

Ex. 1001, 19:24–33. Petitioner contends Ellsberry teaches control ASIC 204, 300, 510, 604, 1102, 1104, 1302 connected to PCB 502, 602 and operatively connected to DDR DRAM memory devices 512. Pet. 55–56. Petitioner further contends the control ASICs receive address and control signals System Address/CMD from processing unit 102. *Id.* at 56. Petitioner further contends the input and address signals are for a write operation to write N-bit-wide write data from the processing unit 102 into one of the multiple N-bit-wide ranks and to output registered address and command signals on bus 220 in response to the received input address and control signals from the processing unit. *Id.* at 56 (citing Ex. 1005 ¶¶ 3, 10, 11, 29, 20, 36, 39, 40, 42, 45, 47, Figs. 2, 3, 5, 6, 8, 11, 13; Ex. 1003 ¶¶ 306–318). Petitioner sufficiently shows that Elsberry teaches limitation [1c1] of claim 1 of the '339 patent.

Limitation [1c2] of claim 1 of the '339 patent recites "wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control

signals." Ex. 1001, 19:33–39. Petitioner contends that Ellsberry teaches that the registered address and control signals on bus 220 cause bank 1 to perform a memory write operation under control of control ASIC 204. Specifically, the control ASIC 204 outputs control signals on bus 210 in response to the input address and control signals from processing unit 102 to cause N-bit-wide write data to be written to Bank 1. Pet. 61 (citing Ex. 1005 ¶¶ 29–31, 39, 42, 52, Figs. 2–4, 8A, 11, 13; Ex. 1003 ¶¶ 319–326). Petitioner sufficiently shows that Ellsberry teaches limitation [1c1] of claim 1 of the '339 patent.

Limitation [1d1] of claim 1 of the '339 patent recites "a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals." Ex. 1001, 19:53–55. Petitioner contends that in Ellsberry switch ASICs 206, 208, 400, 1106, 1304 are byte-wise buffers coupled to PCB 502, 602 and are configured to receive module control signals from the control ASIC on control bus 210. Pet. 65–67 (citing Ex. 1005 ¶¶ 29, 30, 45, 47, Figs. 2–6, 11, 13; Ex. 1003 ¶¶ 327–333). Petitioner shows sufficiently that Ellsberry teaches limitation [1d1] of claim 1 of the '339 patent.

Limitation [1d2] of claim 1 of the '339 patent recites

> wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side.

Ex. 1001, 19:40–49. Petitioner contends that Ellsberry teaches that the byte-wise buffer is the switch ASIC 206, 208 which is connected on a first side to the data buses 230, 232 coupled to DIMM interface 202, 230, DQ(3:0), DQ(7:4) and a second side that is operatively coupled to at least one DDR

DRAM device in each of the multiple N-bit wide banks via data bus 234, 236 (Figs. 2, 4), and "/4" (Fig. 11) and "/8" (Fig. 13). Pet. 68–71. Petitioner further contends Ellsberry teaches a byte-wise data path between data bus 230 and either data bus 234 (Port A) or data bus 236 (Port B) (Figs. 2, 4) or the 8-bit data path between DQ(3:0)/DQ(7:4) (Figs. 11, 13). Pet. 68–71 (citing Ex. 1005 ¶¶ 29, 47, 50, Figs. 2, 5, 6, 11–13; Ex. 1003 ¶¶ 343–347). Petitioner shows sufficiently that Ellsberry teaches limitation [1d2] of claim 1 of the '339 patent.

Limitation [1e] of claim 1 of the '339 patent recites

> wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period.

Ex. 1001, 19:53–61. Petitioner contends that Ellsberry alone or with Halbert teaches limitation [1e] of claim 1. Pet. 73–81. Specifically, Petitioner contends that Ellsberry discloses that switch ASIC 206, 208, 400 includes a control block including read/write logic 406 to control the 8-bit data path between data bus 230 and either data bus 234 (Port A) or data bus 236 (Port B) in response to module control signals on bus 210. *Id.* at 73. Petitioner contends that the byte-wise data path is enabled through Port B and disabled through Port A, or vice versa, for a first time period in accordance with a latency parameter, CAS_n (Fig. 9), to actively drive through bidirectional signal driver 402 or 404 a respective byte-wise section of the N-bit wide write data from the first side, data bus 230, to the second side, data bus 234 or 236, during the first time period, the Posted CAS_n latency parameter, to

avoid bus conflicts. Pet. 73–75 (citing Ex. 1005 ¶¶ 11, 29, 31, 39, 40, 44–46, 50, Figs. 2, 4, 9; Ex. 1003 ¶¶ 348–368).

Petitioner further contends that Halbert teaches using preset latency parameters for timing data transfer bursts and that the data paths are driven only during the data bursts. Pet. 79 (citing Ex. 1006, 1:51, 2:46–60, 6:66–67, 9:55–65, Figs. 3–6; Ex. 1003 ¶ 362).

Patent Owner contends that Petitioner has not identified what in Ellsberry or Halbert meets the claimed "first time period." Prelim. Resp. 32–35. Petitioner identified the claimed "first time period" to be "e.g., the time period for the respective data burst starting in accordance with the 'latency parameter' to avoid bus conflicts." Pet. 74 (emphasis omitted). In addition, Petitioner's declarant testifies that "a Skilled Artisan would have understood that the DQ data lines (and the corresponding DQS strobe lines) of a memory device are driven only 'for a first time period' in accordance with latency parameters including the Posted CAS latency ('AL') and the CAS latency ('CL')." Ex. 1003 ¶ 352 (emphasis omitted). Thus, on this record, we do not agree with Patent Owner's argument.

Patent Owner next argues that Petitioner's expert admits that the data path is enabled for a duration in accordance with a burst length parameter (BL) and that the latency parameter only affects the start of the enablement period. Prelim. Resp. 35–36. The claim language in question is that the "data path is enabled for a first time period in accordance with a latency parameter." Ex. 1001, 19:56–57. Patent Owner does not explain why this claim language must refer to the duration of the first time period, and not the point at which it starts, as Petitioner contends. On this record, we are sufficiently persuaded by Petitioner's argument that enabling the data path for a time period that starts based on the latency parameter teaches "the byte-

wise data path is enabled for a first time period in accordance with a latency parameter." Ex. 1003 ¶ 352.

Patent Owner next contends that Ellsberry does not involve enabling or disabling data paths. Prelim. Resp. 37–43. As Petitioner contends, however, Ellsberry discloses enabling or disabling data paths from one side of a switch ASIC to the other using bidirectional signal drivers 402/404 which enable or disable respective data paths. *See* Pet. 150 (citing Ex. 1005 ¶¶ 46, 57, Fig. 4; Ex. 1003 ¶ 156). Likewise, Halbert's tristate buffers 122, 126, 128 enable or disable data paths through the data interface circuit 120 between the system bus and the memory bus. Ex. 1006, 4:49–5:14, Fig. 4. Thus, we do not agree with Patent Owner's argument.

Patent Owner next asserts that Halbert and the combination do not disclose limitation [1e] of claim 1 because Petitioner did not provide "analysis of what is the latency parameter according to which the data path is enabled for a first time period; nor is there any explanation why . . . Halbert shows that the data paths are enabled for the same 'first time period' during which data is driven." Prelim. Resp. 49–51 (citing Pet. 80–81). As Petitioner points out, however, the '339 patent states "[a]s is known, [the] Column Address Strobe (CAS) latency is a delay time," showing that latency was known, and Petitioner argues that latency was standardized by JEDEC and measured in clock cycles. Reply 1 (citing Ex. 1001, 15:61–66). Patent Owner does not explain why Halbert must teach what the '339 patent states was known. Petitioner further contends that "nothing in the patent or the claims requires the latency to affect the duration." *Id.* at 2–3. Patent Owner does not sufficiently address why the claim language requires latency to relate to the duration of the time period during which data is driven, rather than the start of that time period.

Limitation [1f] of claim 1 of the '339 patent recites

> wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

Ex. 1001, 19:62–67. Petitioner contends that Ellsberry alone or with Halbert teaches limitation [1f] of the '339 patent. Pet. 81–86. Specifically, Petitioner contends Ellsberry alone or with Halbert teaches that the data path through Port A or Port B within bidirectional drivers 402, 404 (Ellsberry Fig. 4) and the control block (Ellsberry Fig. 4) in response to module control signals on bus 210 are configured to enable tristate buffers (Halbert Fig. 4) to drive the byte-wise section of the N-bit wide write data to the respective module lines 234 or 236 (Ellsberry Figures 2, 4) during a first time period corresponding to burst and latency parameters. *Id.* at 81–82 (citing Ex. 1005 ¶¶ 31, 45, Figs. 2, 4, 8A; Ex. 1003 ¶¶ 369–377). Petitioner contends that given the data buses are bidirectional, it would have been obvious to implement Ellsberry's bidirectional drivers 402, 404 (Fig. 4) using tristate buffers. *Id.* at 83 (citing Ex. 1003 ¶¶ 372–373).

To the extent Ellsberry does not sufficiently teach limitation [1f], Petitioner contends that it would have been obvious to implement bidirectional drivers 402, 404 using a similar arrangement with Halbert's tristate buffers. *Id.* at 84–85 (citing Ex. 1005, Fig. 4 (Ellsberry and Halbert combined); Ex. 1006, Fig. 4). Petitioner contends that, to drive the write data onto module data lines 236 on Port B, the control block must enable the tristate buffer in bidirectional driver 404 in the write direction during the first time period. *Id.* at 86 (citing Ex. 1003 ¶ 376).

Patent Owner contends that Petitioner has not presented any competent evidence that a person of ordinary skill in the art would have coupled a tristate buffer to the system bus in order to construct a write path having multiple tristate buffers. Prelim. Resp. 51–53. Patent Owner argues that there is no evidence one would have added an additional tristate buffer coupled to system bus 230 as Petitioner argues. *Id.* at 52. Patent Owner argues that Ellsberry already obtains a single load with its bank switches and signal drivers and that, unlike Ellsberry, Halbert's memory ranks receive the same commands and perform memory operations concurrently. *Id.* at 52–53. Patent Owner contends that Petitioner never explained why a person of ordinary skill in the art would have added redundant functions and combined incompatible implementations with a reasonable expectation of success. *Id.* at 53.

Petitioner contends adding Halbert's tristate buffers to Ellsberry is not redundant because Ellsberry's Figure 4 is not a "single load" embodiment. Pet. 33–35, 44–47. Patent Owner's declarant, however, contends that Ellsberry already discloses presenting a single load, which means that additional hardware is not required and would only add cost without any benefits. Ex. 2001 ¶¶ 81–82. On this preliminary record, we are sufficiently persuaded that using tristate buffers as Petitioner proposes would have involved little more than combining familiar elements according to known methods to yield predictable results. *See KSR*, 550 U.S. at 416; Pet. 33–35, 44–47. As to alleged incompatibility, Halbert teaches that "[*g*]*enerally*, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently. Ex. 1006, 4:57–59 (emphasis added). Halbert's use of the word "generally" means that is not always the case that memory ranks perform memory

operations concurrently. Consequently, we do not agree with Patent Owner's argument.

Patent Owner next contends there is no competent evidence that a person of ordinary skill in the art would have added a tristate buffer to Ellsberry's delayed flip-flops with inputs associated with a write command. Prelim. Resp. 52–57. Patent Owner contends adding a tristate buffer would cause bus conflicts while Petitioner contends a tristate buffer would eliminate them. Ex. 1003 ¶ 260; Ex. 2001 ¶ 88. Patent Owner recognizes, however, that bus conflicts can be avoided using arbitration lines. Ex. 2001 ¶ 88. Patent Owner does not explain why Ellsberry's control ASIC 204 would not be able to generate appropriate control signals via arbitration lines to prevent bus conflicts.

Patent Owner argues that Petitioner has not shown *prima facie* evidence that enablement of tristate buffers was by logic in response to a module control signal. Prelim. Resp. 57. Patent Owner contends Petitioner maps the recited "logic" to Ellsberry's control block (Fig. 4) but has not identified any specific module control signals in response to which the write tristate buffers would be enabled. *Id.* Patent Owner contends none of the signals shown in Ellsberry's Figures 10 to 13 are ones that can reasonably be interpreted as activating (or deactivating) a data port as opposed to signaling for activating (or deactivating) memory banks. *Id.* (citing Ex. 1005, Figs. 10–13; Ex. 2001 ¶¶ 52, 61, 62).

Patent Owner's argument assumes that one of ordinary skill in the art would not have understood how to implement Ellsberry's read/write logic 406 with control lines to appropriately control Halbert's tristate buffers to enable or disable data paths to write data to respective memory banks. Ex. 1005, Fig. 4. Halbert shows control signals that are used to control

tristate buffers 122, 126, 128. Ex. 1006, Fig. 4. Stone teaches that bus conflicts can be avoided with arbitration lines. Ex. 1035, 90, *cited in* Ex. 2001 ¶ 88. With this knowledge, we are sufficiently persuaded, on this record, that a person of ordinary skill in the art would have been capable of implementing logic and control lines appropriately to enable or disable data paths to respective memory ranks.

We determine that Petitioner has shown a reasonable likelihood that claim 1 of the '339 patent is unpatentable as obvious over the combination of Ellsberry and Halbert.

8. Claims 2–10

Claim 2 of the '339 patent depends from claim 1 and recites

> wherein the DDR DRAM devices each has a bit width of 4 bits, wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a respective pair of DDR DRAM devices, and wherein a first subset of the first tristate buffer is enabled for the first time period to drive a first nibble of the respective byte-wise section of the N-bit wide write data to a first subset of the respective module data lines coupled to a first one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit wide rank, while a second subset of the first tristate buffers is enabled for the first time period to drive a second nibble of the respective byte-wise section of the N-bit wide write data to a second subset of the respective module data lines coupled to a second one of the respective pair of DDR DRAM devices in each of at least some of the multiple N-bit wide rank.

Ex. 1001, 20:1–18. Petitioner contends that Ellsberry alone or with Halbert teaches the limitations of claim 2. Pet. 86–89 (citing Ex. 1005 ¶¶ 49, 51,52, Figs. 2, 6, 11; Ex. 1006, Fig. 4; Ex. 1003 ¶¶ 379–391). Patent Owner contends that Petitioner does not explain why two sets of drivers connected to the same port A could be and would be driven at the same time. Prelim. Resp. 58–59. However, Petitioner relies on Ellsberry's Figure 11, which

appears to teach two sets of drivers connected to port A, and two sets of drivers connected to port B, to drive signals into respective memory ranks. Although Patent Owner points to Petitioner's discussion of Ellsberry's Figure 4 and alleges it is inconsistent (Pet. 32–33), it teaches the concept of having two ports. Ellsberry's Figure 11 is simply a modification of Ellsberry's Figure 4 which splits each port into two four-bit nibbles. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 2 of the 339 patent.

Claim 3 depends from claim 2 and recites

> wherein the byte-wise data path further includes a set of write buffers configurable to receive the respective byte-wise section of the N-bit wide write data from the respective set of data signal lines before the first tristate buffers regenerate and drive the respective byte-wise section of the N-bit wide data to the second side of the each respective byte-wise buffer.

Ex. 1001, 20:19–25. Thus, claim 3 recites write buffers arranged in the byte-wise data path before tristate buffers. Ex. 1001, 20:1925. Petitioner contends that Ellsberry alone or with Halbert teaches this feature. Pet. 89–93 (citing Ex. 1005 ¶¶ 12, 27, 45, 50, claim 2, Figs. 2, 4, 11; Ex. 1003 ¶¶ 395–407). Patent Owner contends that Petitioner maps the set of write buffers to either Ellsberry's write buffer in driver 404 or a buffer coupled to bus 230. Prelim. Resp. 60. We understand Petitioner to identify the set of write buffers connected to 230 and tristate buffers connected to either 402 or 404, depending upon which port is enabled, by modifying Ellsberry with Halbert's teachings. Petitioner has shown sufficiently that the combination of Ellsberry and Halbert teaches the write buffers of claim 3.

Claim 4 depends from claim 3 and recites "wherein each of the write buffers is comparable to an input buffer on one of the DDR DRAM devices

such that the each respective byte-wise buffer presents to the memory controller one DDR DRAM device load during the memory operation." Ex. 1001, 20:26–30. Petitioner contends that Ellsberry alone or with Halbert teaches claim 4. Pet. 93–95 (citing Ex. 1005 ¶¶ 12, 27, 31, 46, 50, Figs. 2, 4, 6, 11; Ex. 1003 ¶¶ 408–415). Patent Owner does not dispute Petitioner's contentions concerning claim 4. Petitioner has shown sufficiently that Ellsberry alone or combined with Halbert teaches claim 4.

Claim 5 depends from claim 1 and recites "wherein the DDR DRAM devices each has a bit width of 8 bits, and wherein the at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks includes a single DDR DRAM device." Ex. 1001, 20:31–35. Petitioner contends that Ellsberry teaches claim 5. Pet. 95–96 (citing Ex. 1005 ¶¶ 10, 37, 52, Figs. 2, 7, 13; Ex. 1003 ¶¶ 416–420). Patent Owner does not dispute Petitioner's contentions concerning claim 5. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 5.

Claim 6 depends from claim 1 and recites "wherein the logic is configurable to enable the first tristate buffers at a beginning of the first time period and to disable the first tristate buffers at an end of first time period." Ex. 1001, 20:36–39. Petitioner contends that Ellsberry alone or with Halbert teaches claim 6. Pet. 97 (citing Ex. 1005; Ex. 1003, Fig. 4; Ex. 1003 ¶¶ 421–423). Patent Owner contends that Halbert's buffer 122 defaults to receiver and Halbert's registers 126 and 128 default to drivers except when read commands are detected. Prelim. Resp. 61–62 (citing Ex. 1006, 5:30–36). Patent Owner argues, therefore, that "Halbert does not teach the recited timing relationship." Prelim. Resp. 62. On this record, we are sufficiently persuaded by Petitioner's contentions for claim 6 given the language of the claim, which recites that "the logic is configurable to" operate with a

particular timing relationship, rather than "configured to" so operate.

Claim 7 depends from claim 1 and recites "wherein the module controller is configured to use the module control signals to control timing of the first time period in accordance with the latency parameter." Ex. 1001, 20:40–43. Petitioner contends Ellsberry alone or with Halbert teaches claim 7. Pet. 98–99 (citing Ex. 1005, Fig. 4 (modified by Petitioner); Ex. 1003 ¶¶ 424–426). Patent Owner argues that a module control signal is one outputted by the module controller "in response to at least some of the input address and control signals." Prelim. Resp. 62 (citing Ex. 1001, 19:36–39). Patent Owner argues that the latency parameter relied on by Petitioner is "passed thru as received from the Host." *Id.* (citing Ex. 1005, Fig. 9). Patent Owner does not explain, however, why the latency parameter is not a control signal that is "passed thru" the module controller as a module control signal. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 7.

Claim 8 depends from claim 1 and recites "wherein the registered address and control signals include rank select signals, the rank select signals including one rank select signal for each of the multiple N-bit-wide ranks, and wherein the rank select signal received by the first N-bit-wide rank is different from the rank select signal received by any other N-bit-wide rank of the multiple N-bit-wide ranks." Ex. 1001, 20:44–50. Petitioner contends Ellsberry alone or with Halbert teaches claim 8. Pet. 99–104 (citing Ex. 1005 ¶¶ 11, 30, Figs. 2, 11, 13; Ex. 1003 ¶¶ 435–438). Patent Owner does not separately dispute Petitioner's showing for claim 8.

Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 8.

Claim 9 depends from claim 1 and recites "wherein each of the respective module data lines is configured to carry data from the memory controller to a corresponding memory device in each of the multiple N-bit-wide ranks during the memory write operation." Ex. 1001, 20:51–55. Petitioner contends that Ellsberry alone or with Halbert teaches claim 9. Pet. 104–105 (citing Ex. 1005 ¶¶ 11, 30, Figs. 2, 11, 13; Ex. 1003 ¶¶ 435–438). Patent Owner does not separately dispute Petitioner's showing for claim 9. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 9.

Claim 10 recites

> wherein: the module controller is further configurable to receive from the memory controller via the address and control signal lines additional input address and control signals for a memory read operation to read N-bit-wide read data from the memory controller from a second N-bit-wide rank of the multiple N-bit-wide ranks, and to output additional registered address and control signals in response to the additional input address and control signals; the second N bit-wide rank is configurable to output the N bit-wide read data associated with the memory read operation in response to at least some of the additional registered address and control signals; the module controller is further configurable to output additional module control signals in response to the additional input address and control signals; the logic in the each respective byte-wise buffer is further configurable to control the byte-wise data path in response to the additional module control signals, wherein the byte-wise data path is enabled for a second time period to actively drive a respective byte-wise section of the N bit wide read data associated with the memory read operation from the second side to the first side during the second time period in response to the additional module control signals; the byte-wise data path further includes second tristate buffers configurable to be enabled by the logic to drive the respective byte-wise section of the N-bit wide read data to the respective set of data signal lines during the second time period; and the second tristate buffers

> are disabled during the first time period and the first tristate buffers are disabled during the second time period.

Ex. 1001, 20:56–21:22. Petitioner contends that Ellsberry alone or with Halbert teaches claim 10. Pet. 105–108 (citing Ex. 1005 ¶¶ 3, 10, 11, 29, 31, 40, 45, 46, 50, Figs. 2, 4, 8, 9, 11, 13; Ex. 1006 5:66–6:65, Figs. 3, 5, 6; Ex. 1003 ¶¶ 439–449; Ex. 1003 ¶¶ 441–445, 447). Patent Owner argues that Petitioner has not explained why Halbert's registers and buffers are enabled during the period when read data is actively driven in accordance with a latency parameter (as opposed to MQDS, RDQS signals). Patent Owner does not adequately point out the claim language that supports its argument. On this record, Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 10.

9. Claim 11

Petitioner contends Ellsberry alone or with Halbert teaches all limitations of claim 11. Pet. 108–115. Petitioner contends claim 11 is similar to claim 1 and recites a pair of 4-bit memory devices, as in claim 2. Pet. 108–115 (citing Ex. 1005, Figs. 2, 6, 11; Ex. 1003 ¶¶ 450–490). Patent Owner contends that its criticism of claim 1 applies equally to claim 10. Prelim. Resp. 63. Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches all limitations of claim 11, and we do not agree with Patent Owner's arguments for the same reasons stated for claim 1.

10. Claims 12–17

Petitioner contends that Ellsberry alone or with Halbert teach all limitations of claims 12–17 for similar reasons as stated for previously discussed claims. Pet. 115–116 (citing Ex. 1003 ¶¶ 488–511). Patent Owner presents similar arguments for these claims as for previous claims. Prelim. Resp. 63–64. We similarly find that Petitioner shows sufficiently

that Ellsberry alone or with Halbert teaches all limitations of these claims.

11. Claim 18

Petitioner contends that Ellsberry alone or with Halbert teaches the limitations of claim 18 "for the same reasons as claims 6 . . . and 10." Pet. 116 (citing Ex. 1003 ¶¶ 512–514). Patent Owner argues that claim 6 recites a "completely different limitation" and that, "[t]o the extent Petitioner meant to apply claim 10 analysis, additional comments for claim 10 also apply to claim 18." Prelim. Resp. 64. Petitioner, however, did refer claim 10. *See* Pet. 116. As with claim 10, on this record, Petitioner has shown sufficiently that Ellsberry alone or with Halbert teaches claim 18.

12. Claim 19–35

For claims 19–35, Petitioner refers to its analysis for previously-discussed claims and addresses differences in subject matter. Pet. 116–145. Patent Owner raises various arguments, some of which refer back to arguments made for other claims and some of which are different. Prelim. Resp. 64–69. For example, for claim 22, Patent Owner argues that Petitioner relies on Ellsberry's OCD but does not explain how the limitation of the claim is met. Prelim. Resp. 65–66. Patent Owner, however, does not address Petitioner's argument that a person of ordinary skill in the art would have been motivated to set the load consistent with JEDEC standards. *See* Pet. 122–123. On this record, we determine that Petitioner has sufficiently shown how the combination of Ellsberry and Halbert renders obvious the subject matter of claims 19–35.

IV. CONCLUSION

We determine under the *Advanced Bionics* framework that, although Ellsberry and Halbert were considered individually during examination of

the '912 patent, Petitioner has shown that the Examiner erred in a manner material to patentability. Accordingly, we decline to exercise our discretion to deny institution under § 325(d).

Petitioner has shown a reasonable likelihood that at least one challenged claim would have been obvious over Ellsberry alone or in combination with Halbert, and we institute inter partes review for all of challenged claims 1–35 on all asserted challenges. *See SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348 (2018).

V. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claim 1–35 of the '339 patent is hereby instituted on the grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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